Compal Confidential

HGW51 Schematics Document

AMD/Sempron/ATI RS482M/SB450

2005 / 08 / 18 Rev:0.3 For C test

Security Classification	Compal Secret Data		
Issued Date	2005/05/09	Deciphered Date	2006/03/08

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Title	Cover Sheet	
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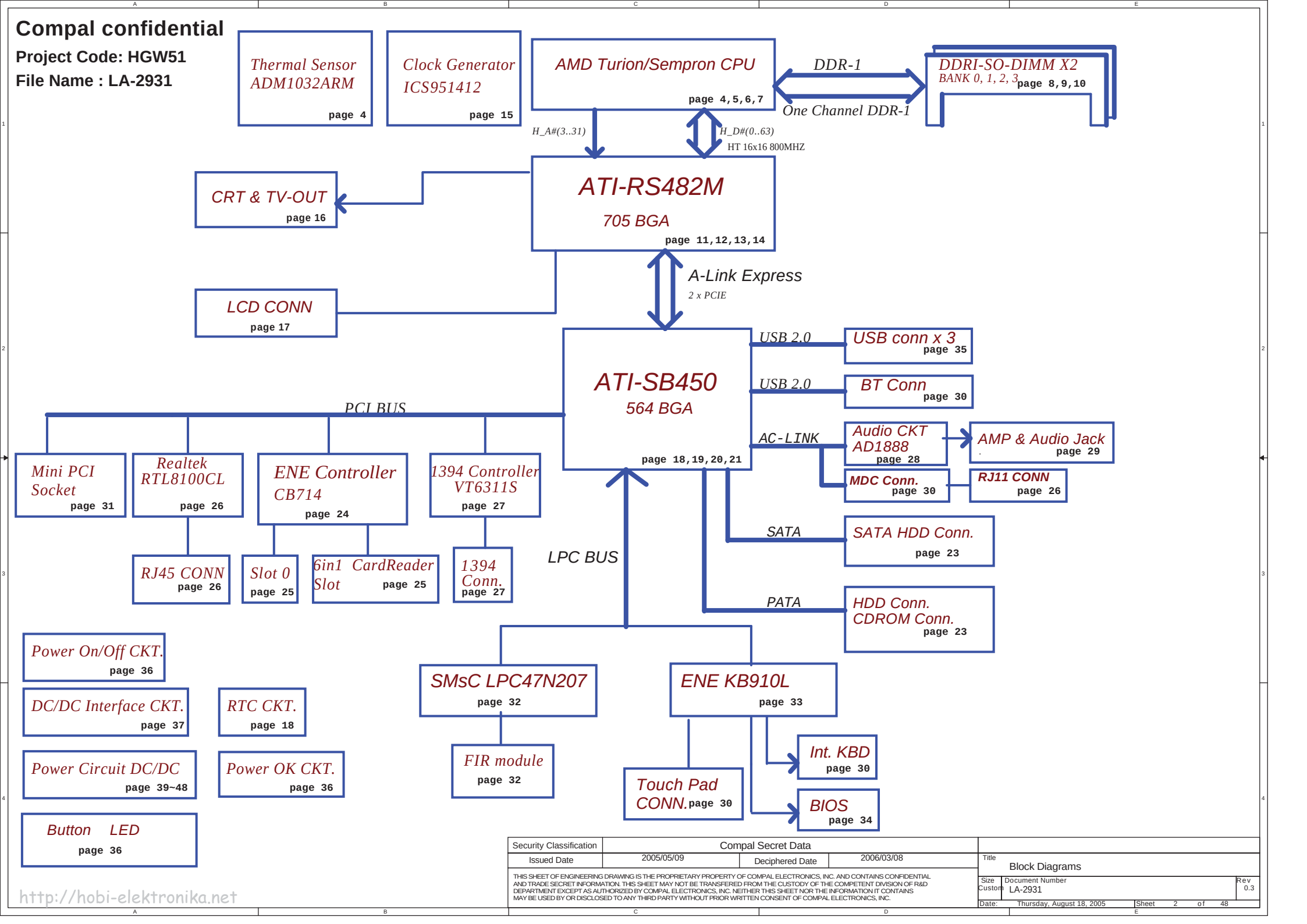
Project Code: HGW51

File Name : LA-2931



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Title	Block Diagrams		
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Voltage Rails

Power Plane	Description	S1	S3	S4/ S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+DDRVTT	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+DDRVCC	1.8V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5VMOD	5V switched power rail for Module Bay	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQE/PIRQH
1394	AD16	0	PIRQE
SD	AD20	2	PIRQE/PIRQH
Mini-PCI	AD18	1	PIRQF
LAN	AD22	3	PIRQG

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
(24C04)	1011 000Xb

EC SM Bus2 address

Device	Address
ADM1032	1001 110X b

SB450 SM Bus address

Device	Address
Clock Generator (ICS 951412AGT)	1101 001Xb
DDRII DIMM0	1001 000Xb
DDRII DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra / Rc	100K +/- 5%

Board ID	Rb / Rd	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure

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Title	Notes		
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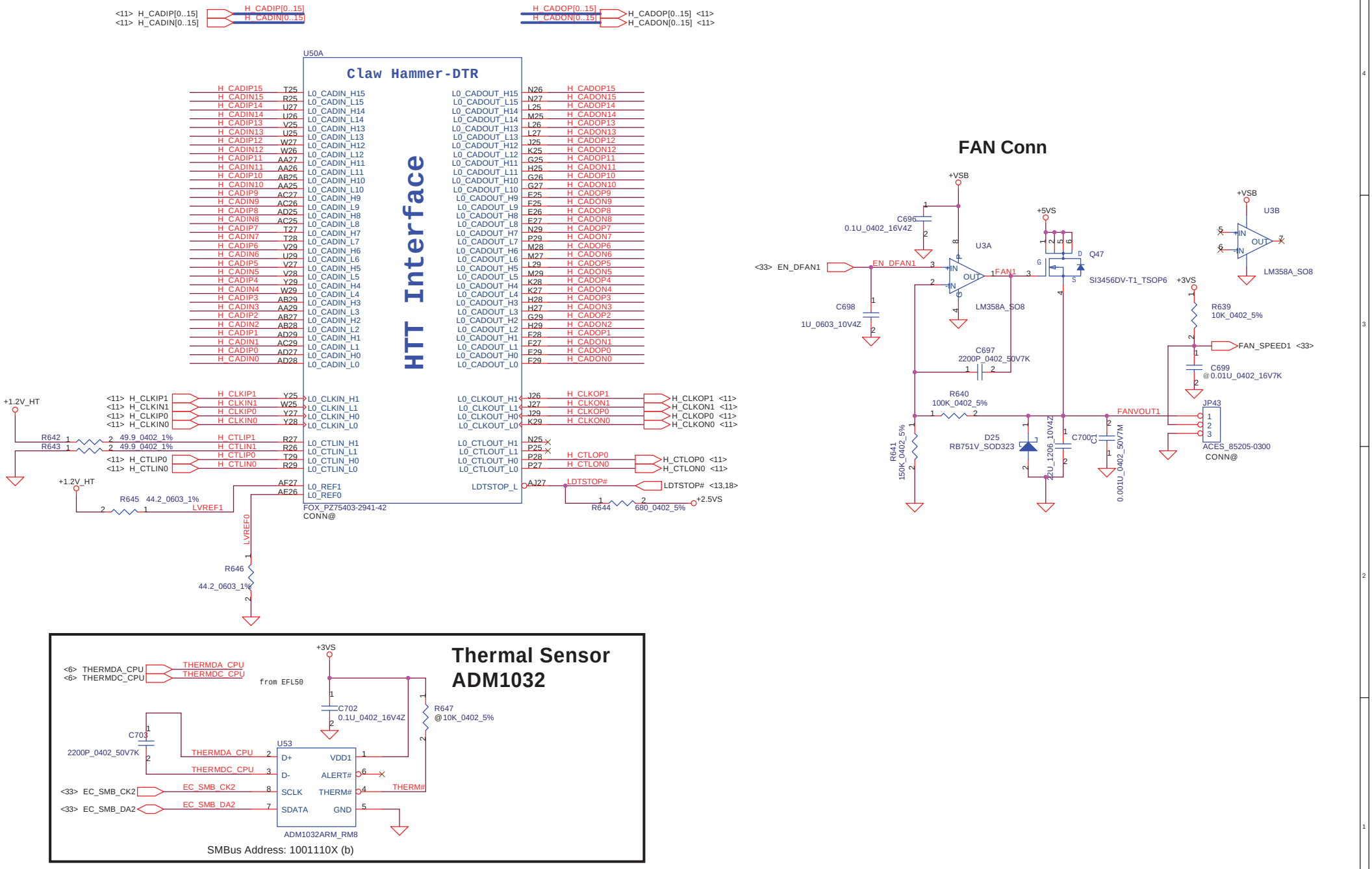

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Title	Claw Harmmer CPU (Host Bus)	
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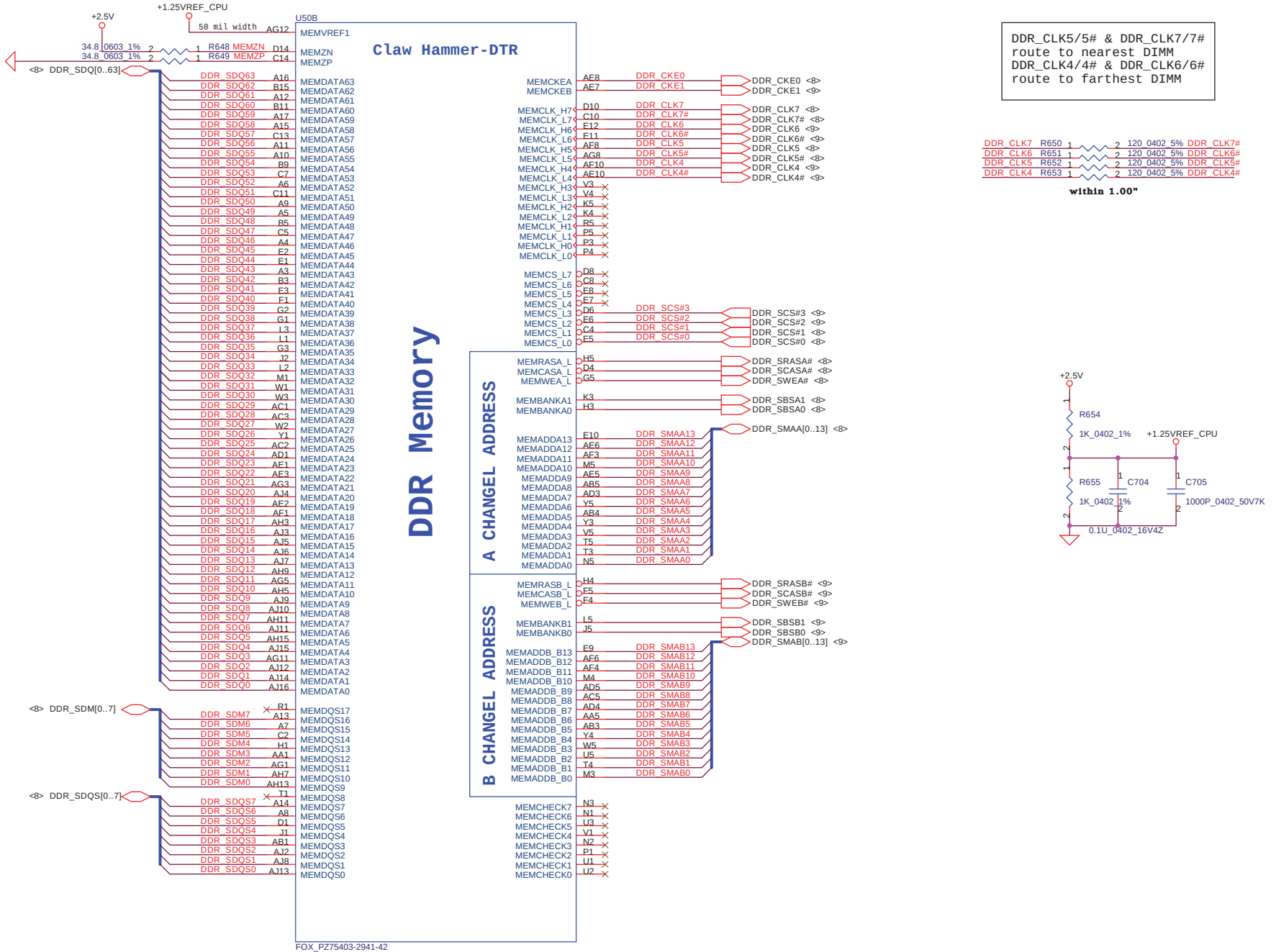

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Title	Claw Harmmer (Memory Bus)		
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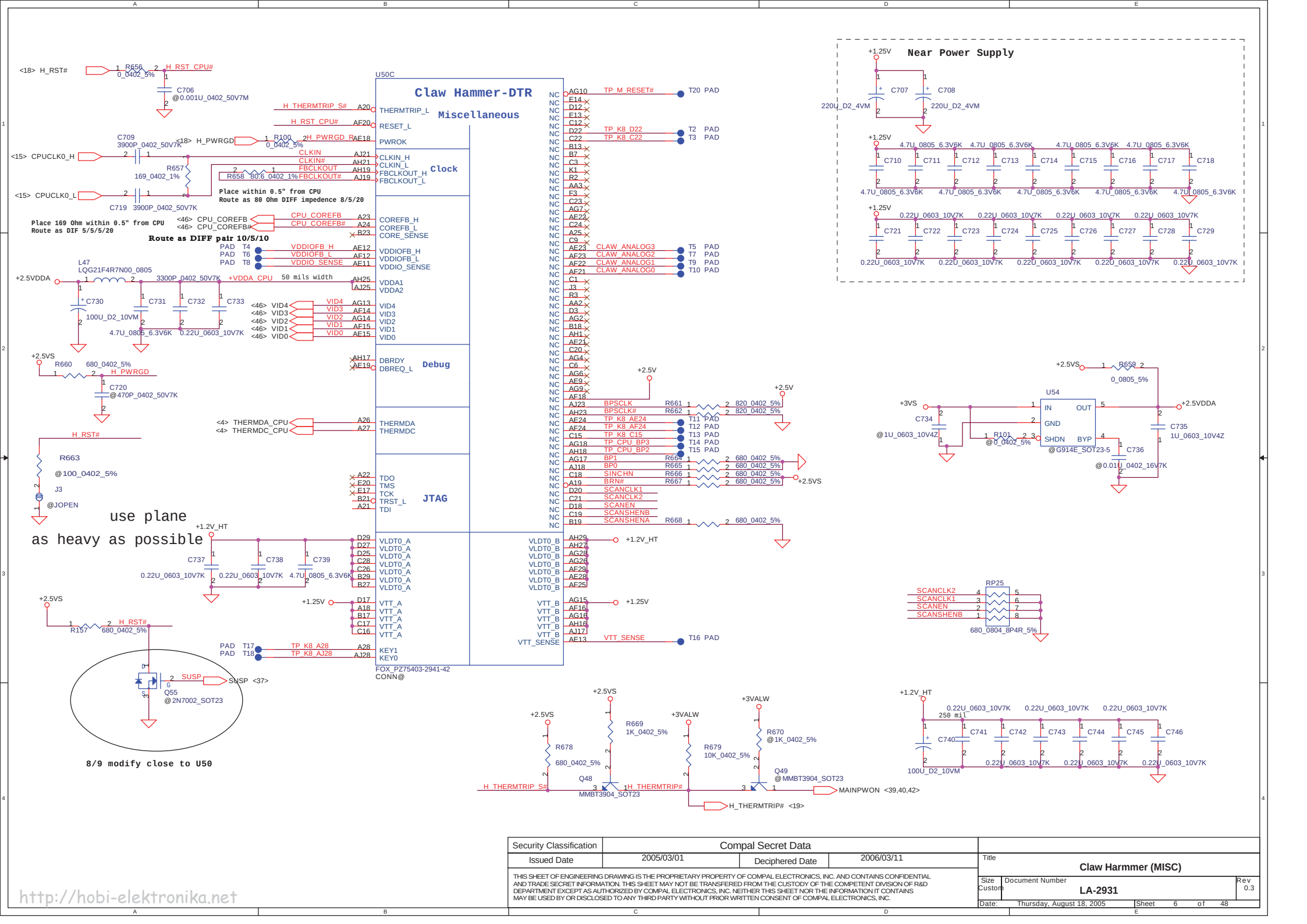

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Title	Claw Harmmer (MISC)		
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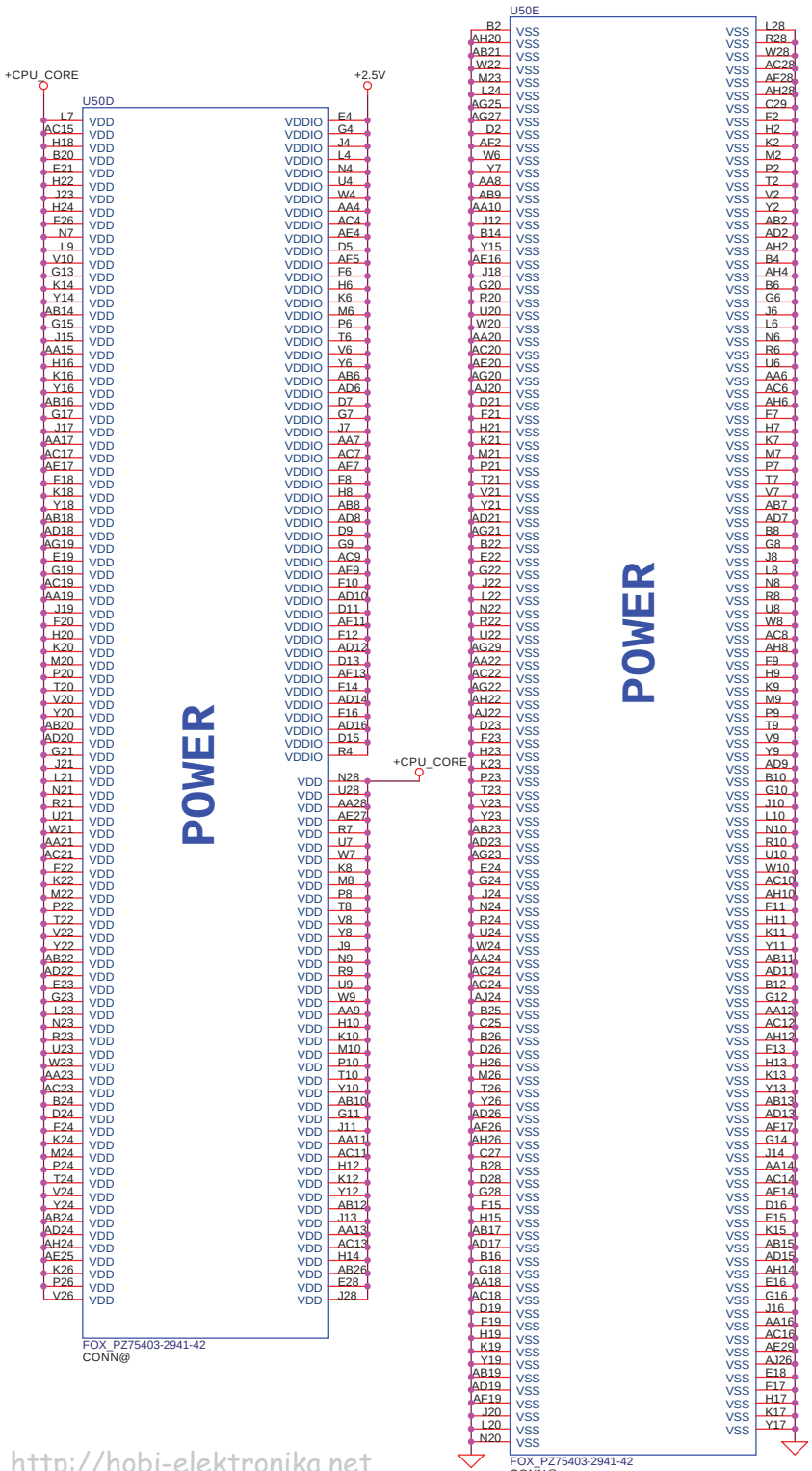
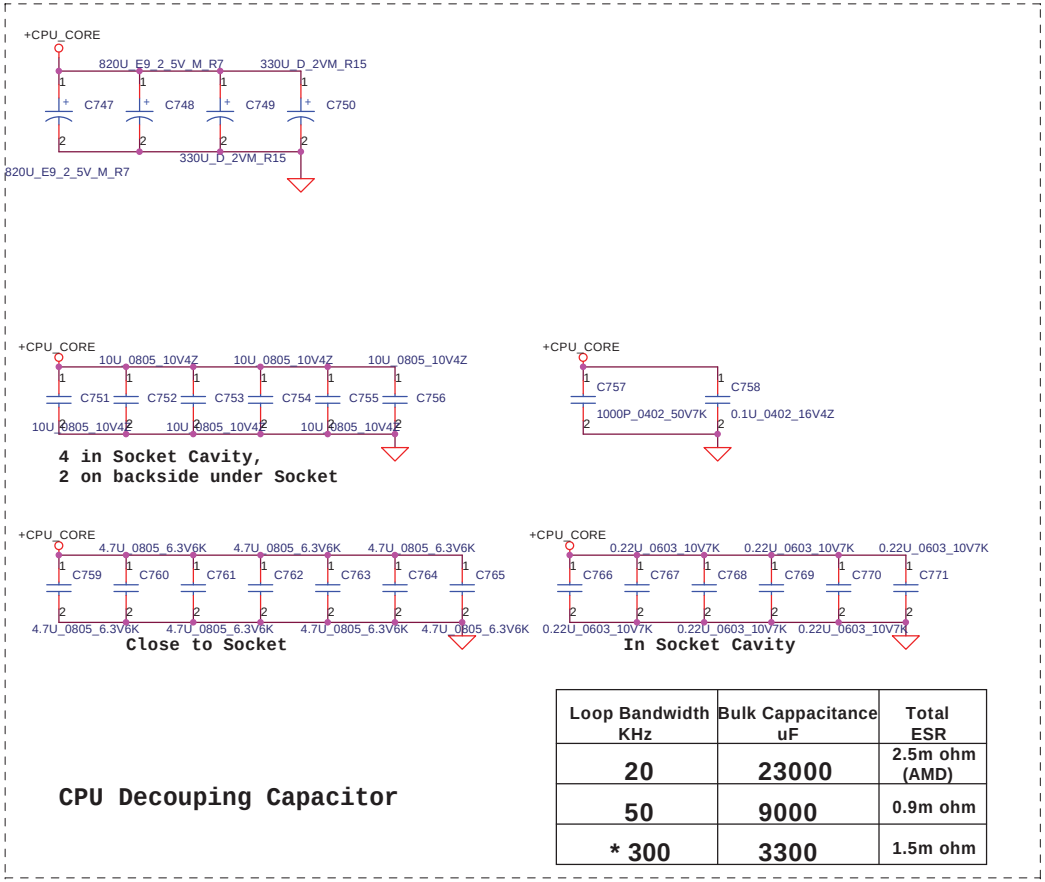
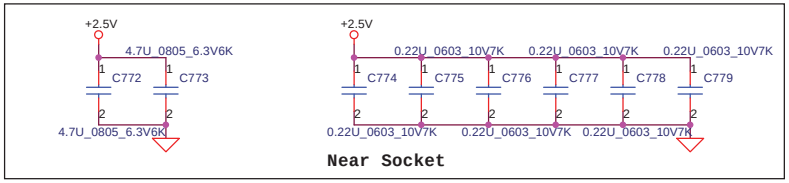




Loop Bandwidth KHz	Bulk Cappacitance uF	Total ESR
20	23000	2.5m ohm (AMD)
50	9000	0.9m ohm
* 300	3300	1.5m ohm



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Title: Claw Harmmer (Power & Ground)

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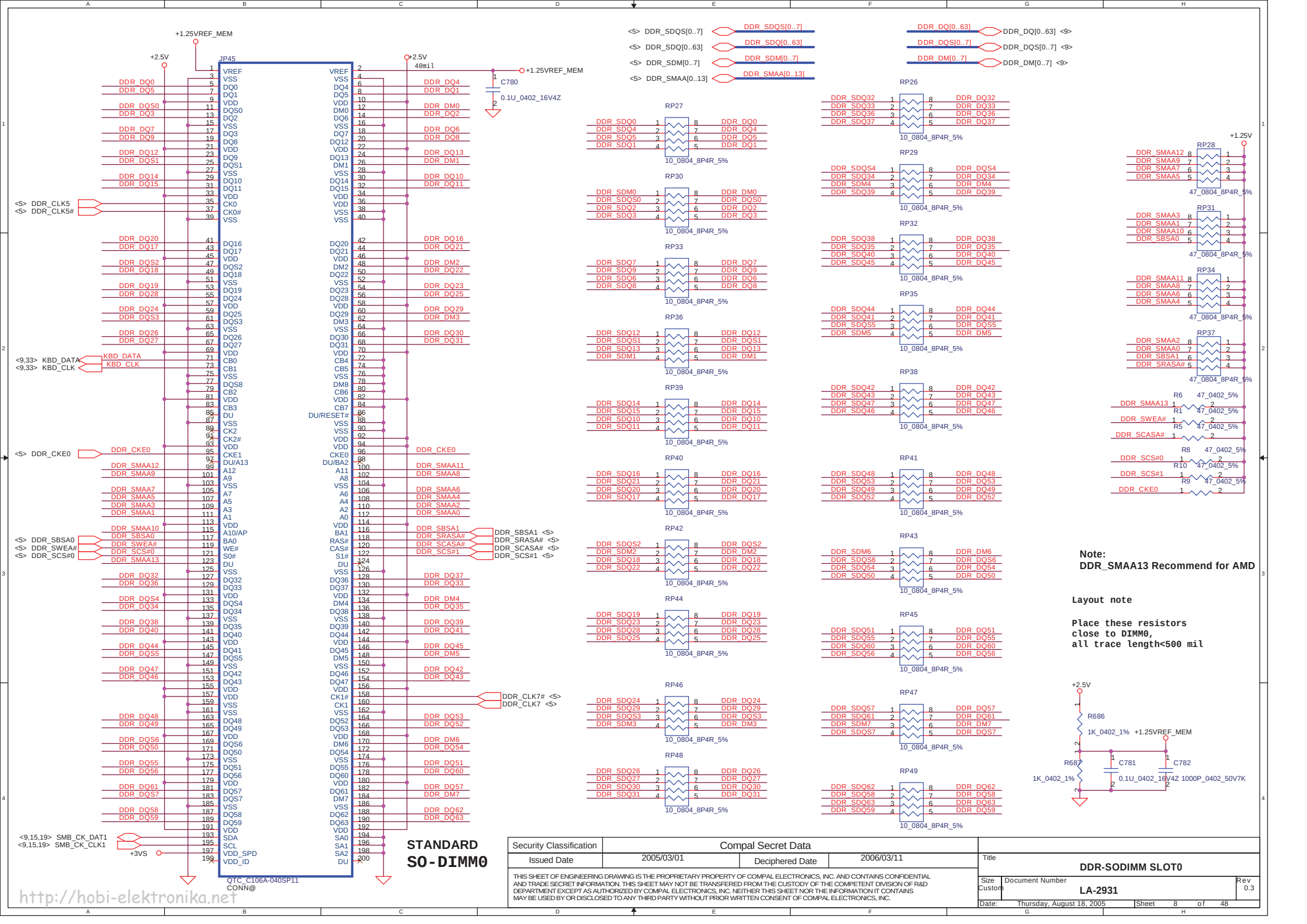

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Title	DDR-SODIMM SLOT0		
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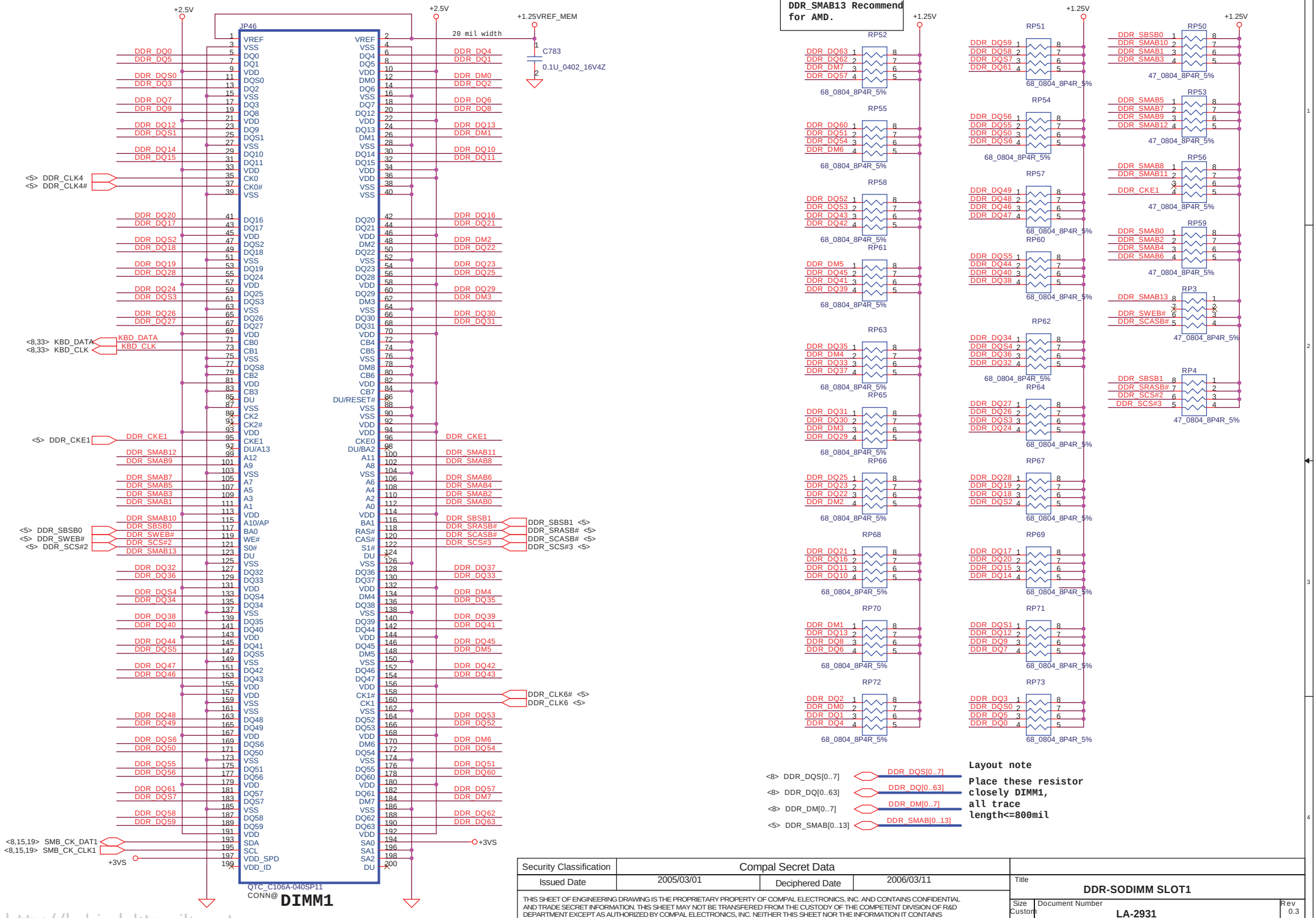

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Title: DDR-SODIMM SLOT1

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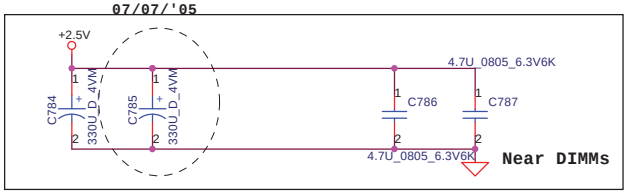
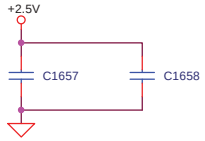
07/07/'05



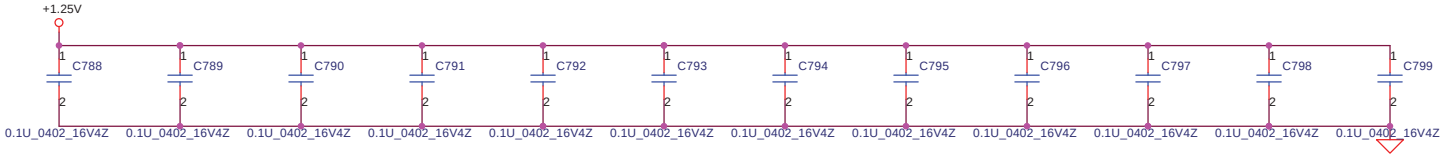


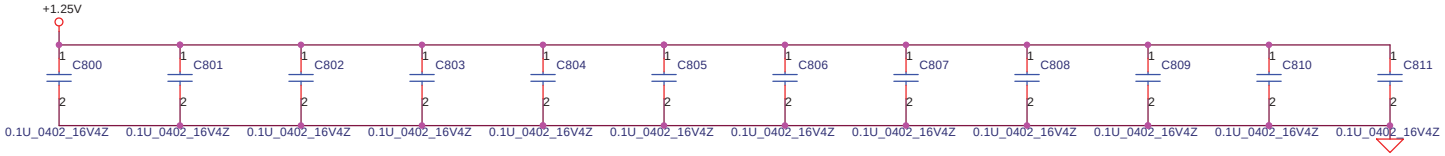
@100P_0402_25V8K @100P_0402_25V8K

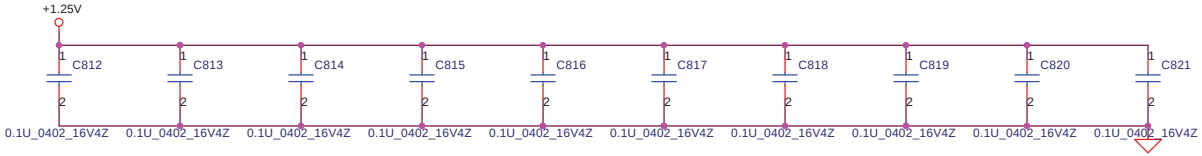
Please Close to DDR_CLK4/5 via hole

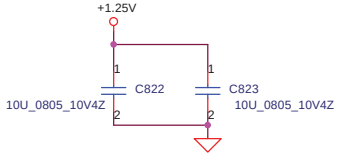
Layout note :

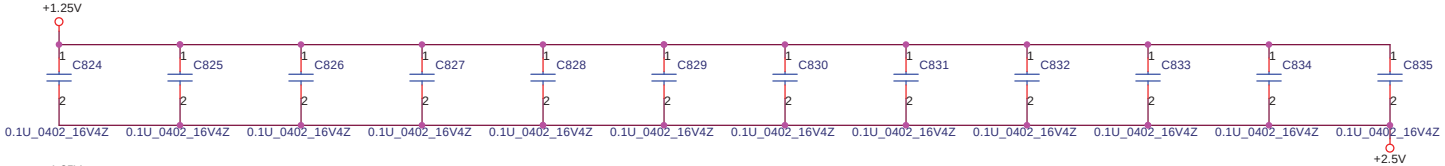
Place one cap close to every 2 pull up resistors termination to +1.25V

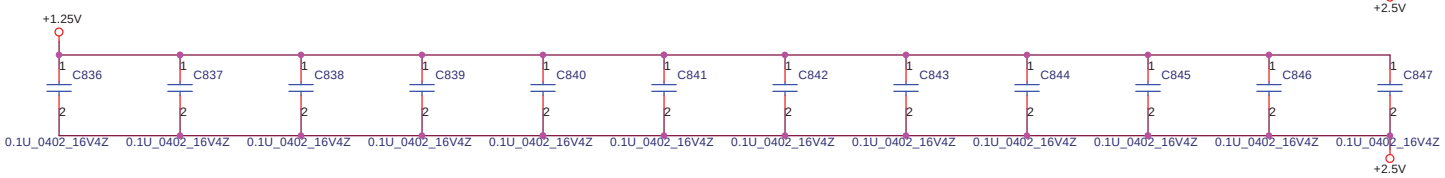


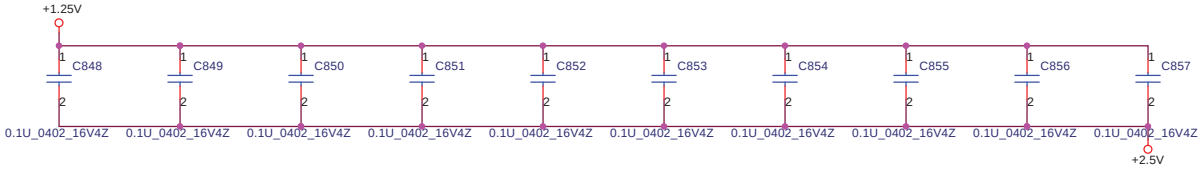












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Title	DDR SODIMM Decoupling		
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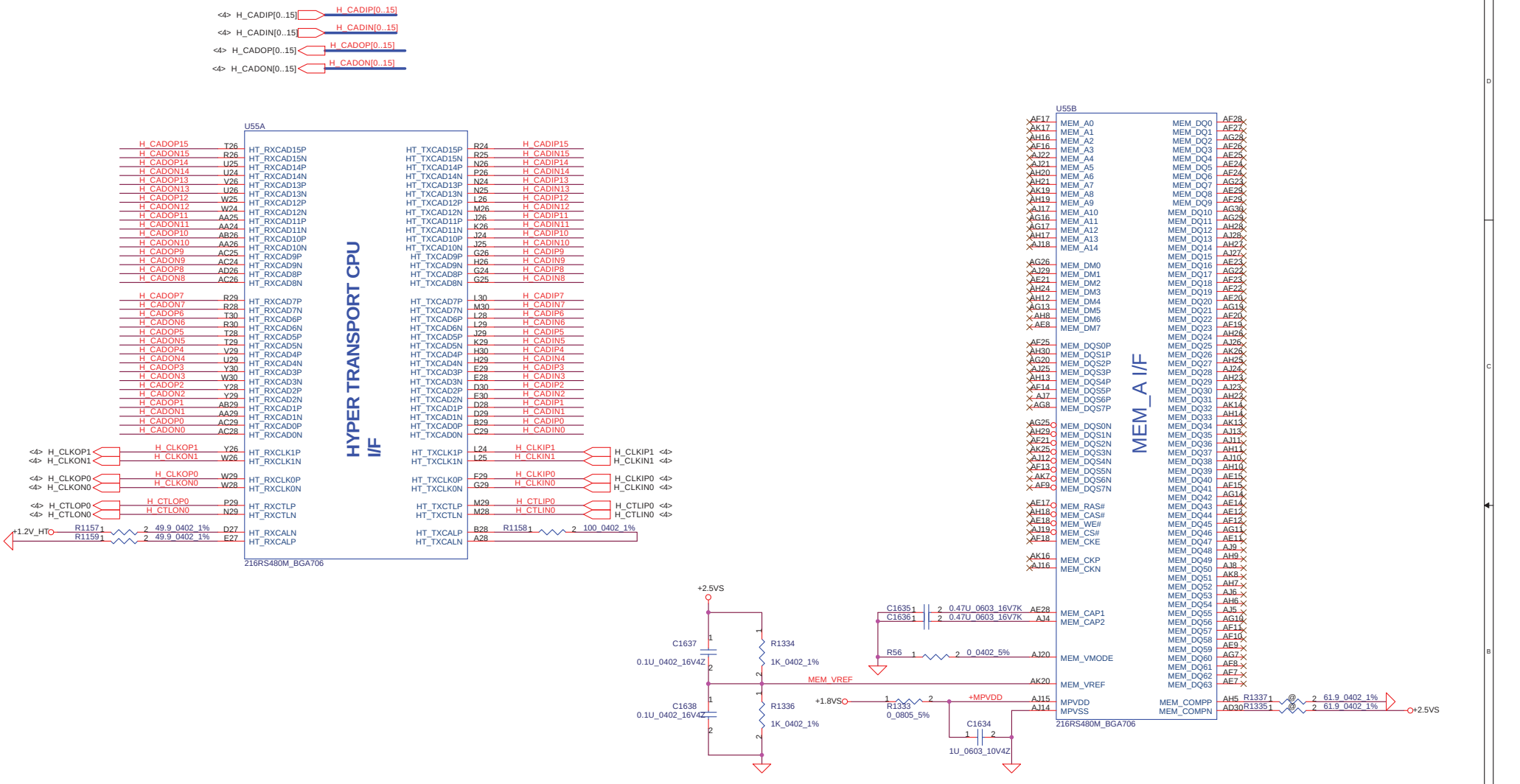

MEM_VREF , MPVDD (20mils)

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Title	RS480M-HT/VMEM		
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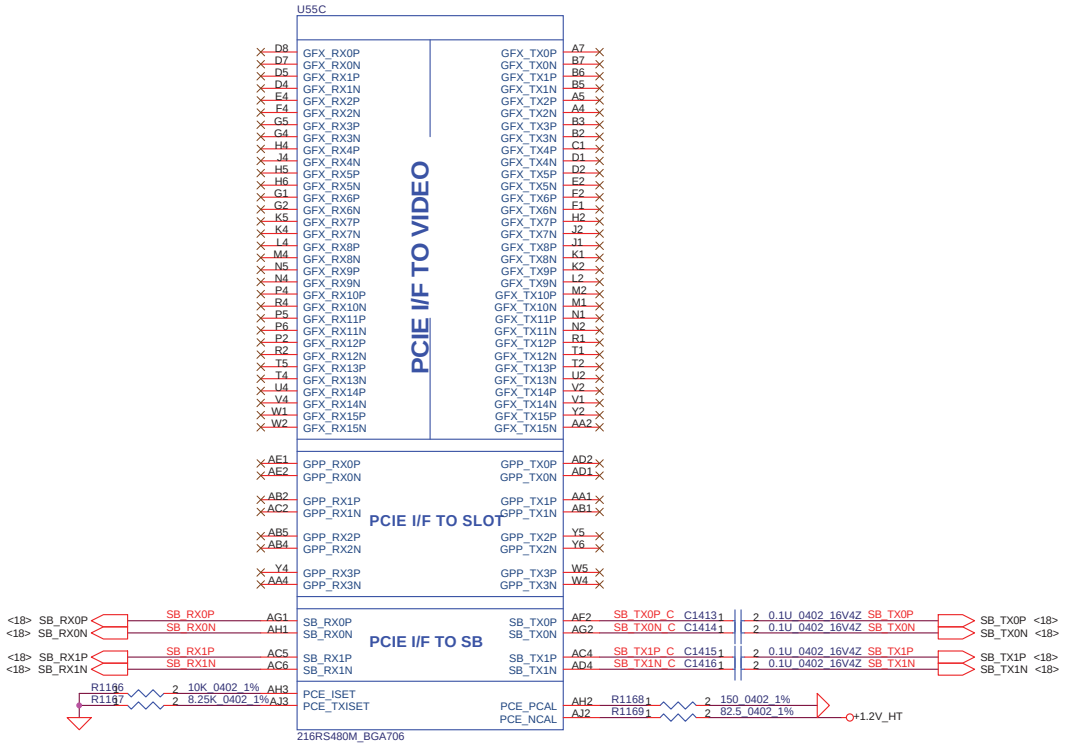

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Title: **RS480M PCIE/DVI Controller**

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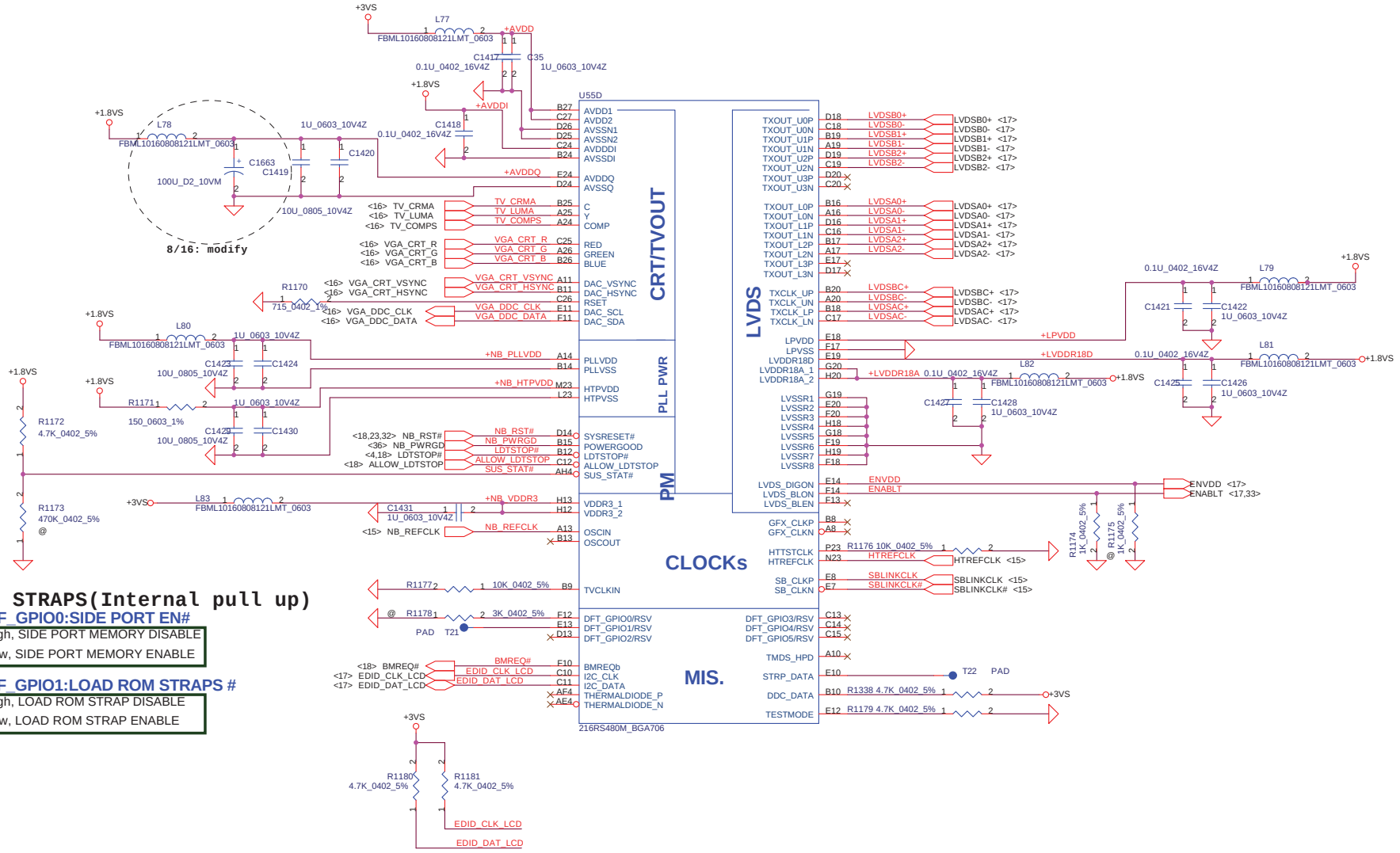
AVDD , AVDDI , AVDDQ , +NB_PLLVDD , +NB_HTPVDD
+NB_VDDR3 , LPVDD , LVDDR18D , LVDDR18A (20mils)



NB STRAPS(Internal pull up)

DEF_GPIO0:SIDE PORT EN#

High, SIDE PORT MEMORY DISABLE
Low, SIDE PORT MEMORY ENABLE

DEF_GPIO1:LOAD ROM STRAPS #

High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE

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Issued Date	2005/03/01	Deciphered Date	2005/04/06

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Title: **RS480M VIDEO_IF/CLOCK GEN**

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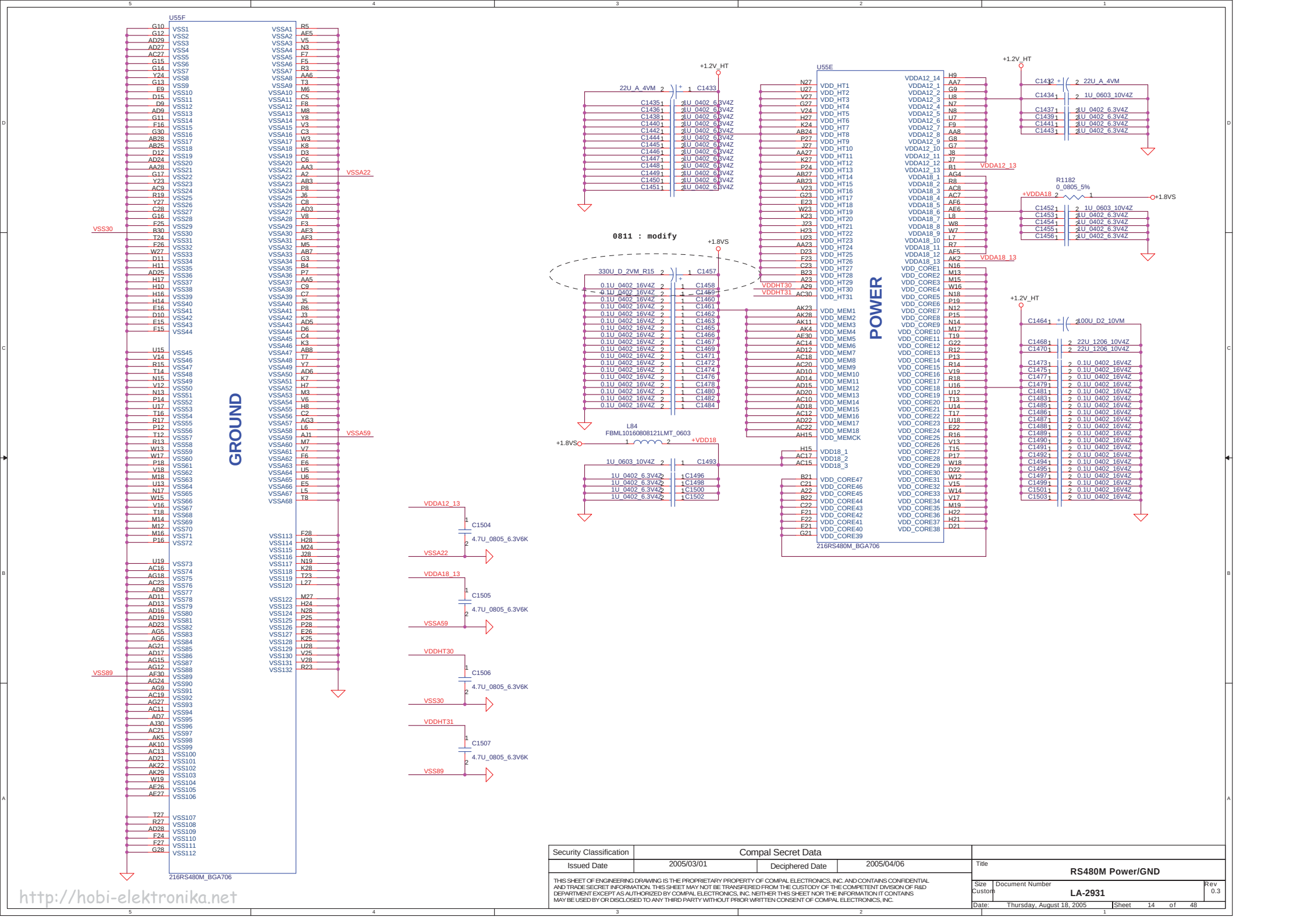

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Title	RS480M Power/GND		
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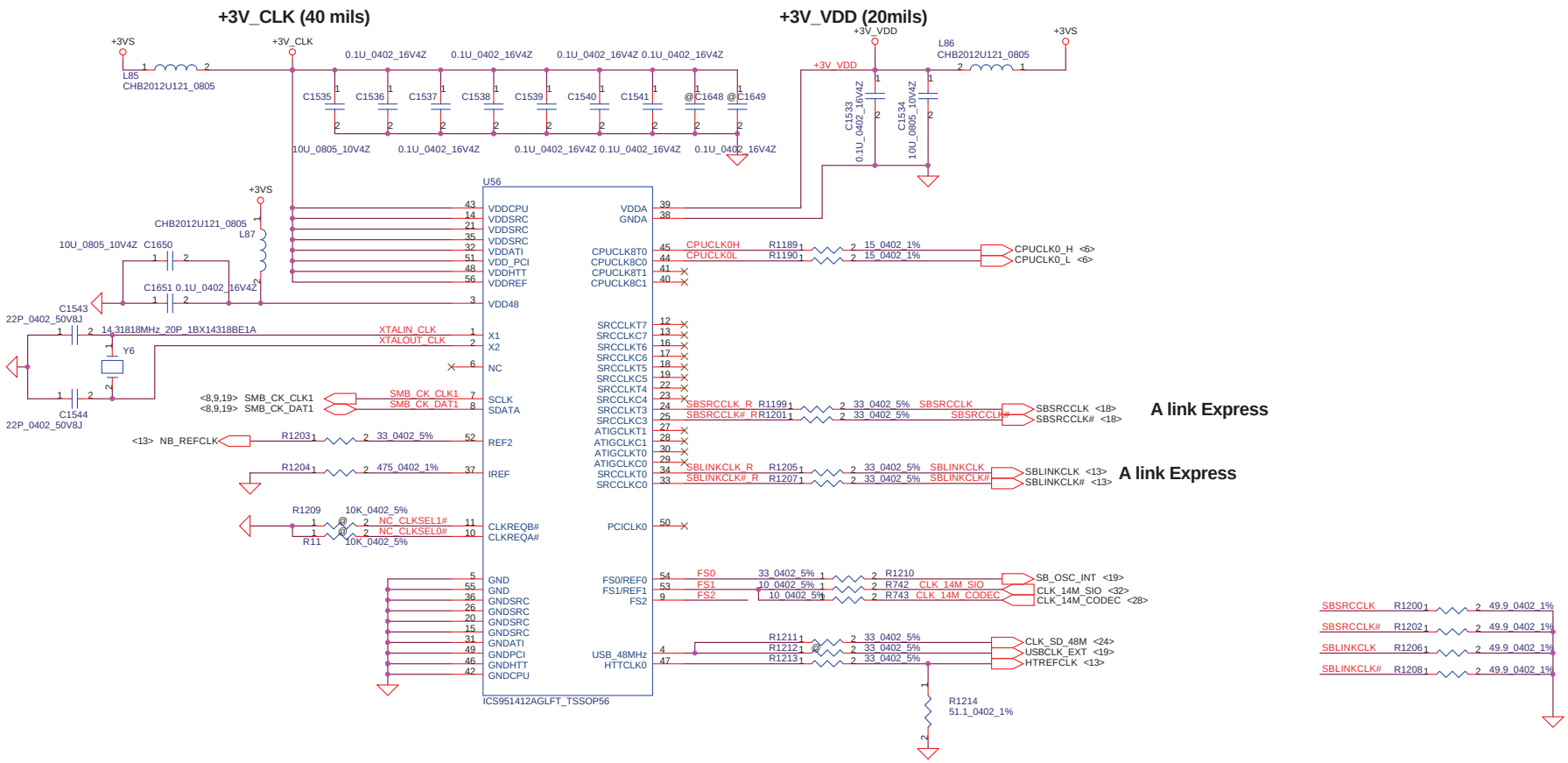

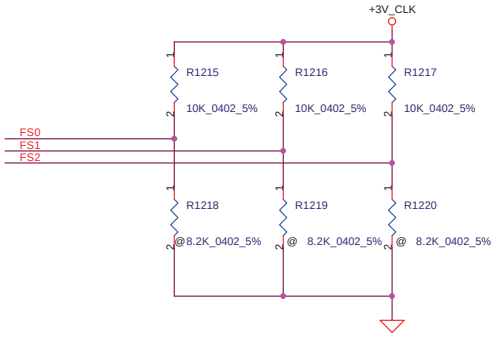

EXT CLK FREQUENCY SELECT TABLE(MHZ)

	FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
	0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
	0	0	1	X	100.00	X/3	X/6	48.00	Reserved
	0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
	0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
	1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
	1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
*	1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

Security Classification	Compal Secret Data		
Issued Date	2005/03/01	Deciphered Date	2005/04/06

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Title	Clock Generator		
Size: Custom	Document Number: LA-2931		Rev: 0.3
Date: Thursday, August 18, 2005	Sheet 15 of 48		

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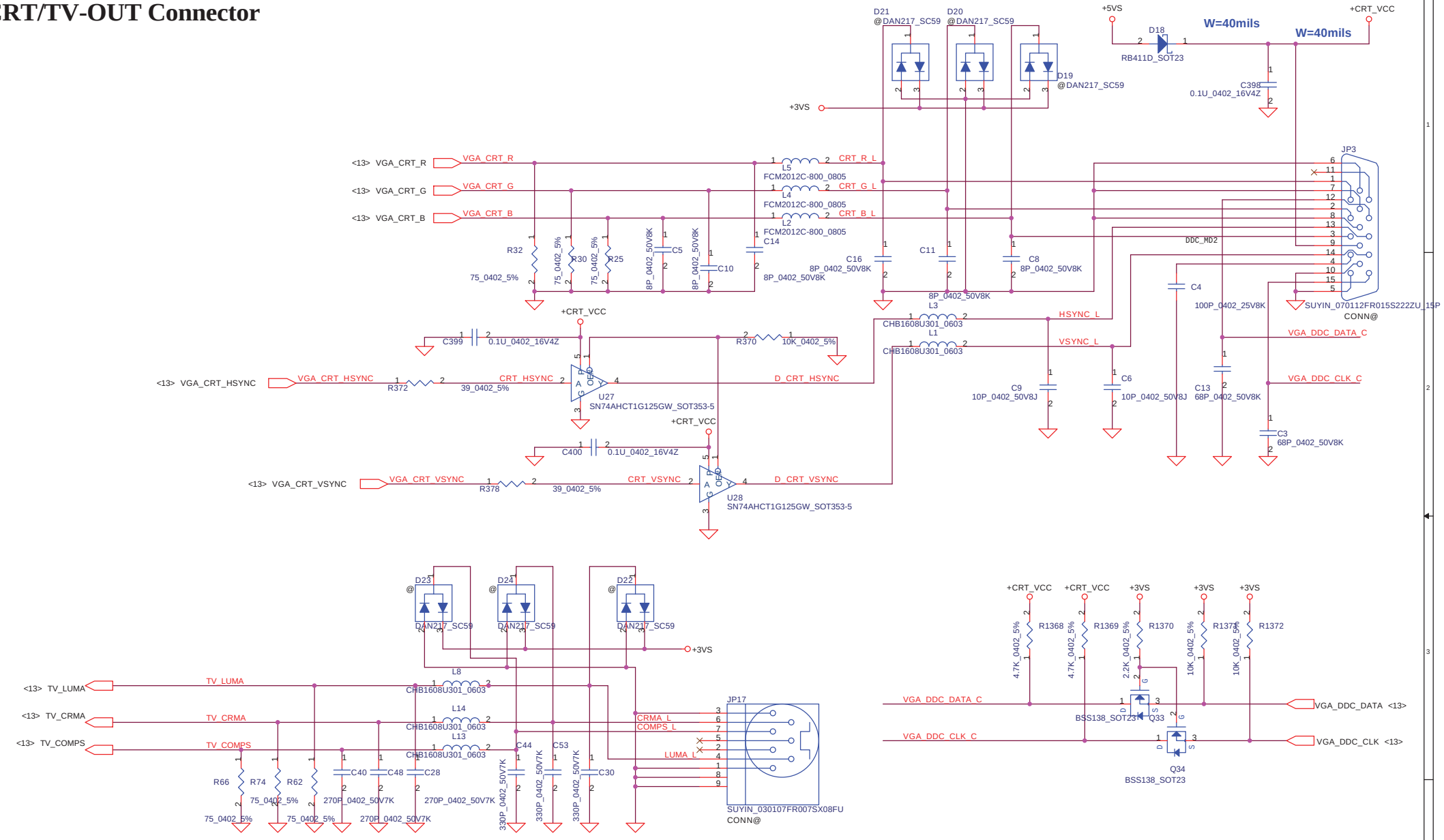
CRT/TV-OUT Connector



Security Classification	Compal Secret Data		
Issued Date	2005/03/01	Deciphered Date	2005/04/06

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Title	TV_OUT/CRT CONN		
Size Custom	Document Number LA-2931		Rev 0.3
Date: Thursday, August 18, 2005	Sheet 16 of 48		

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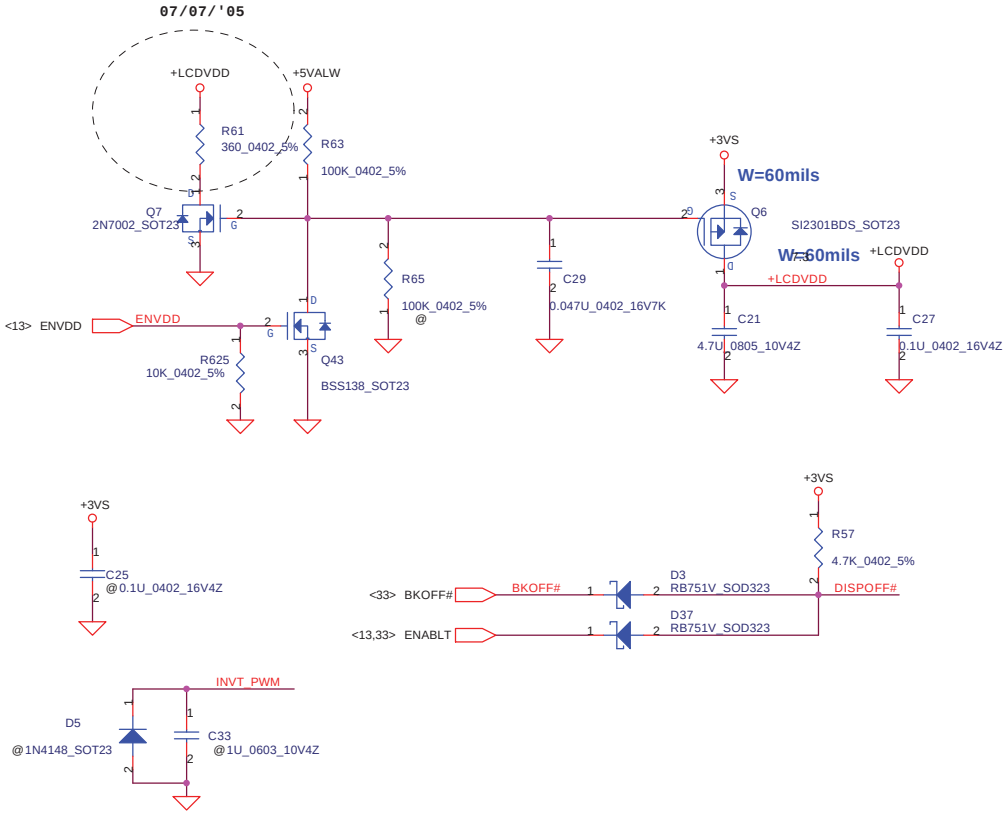
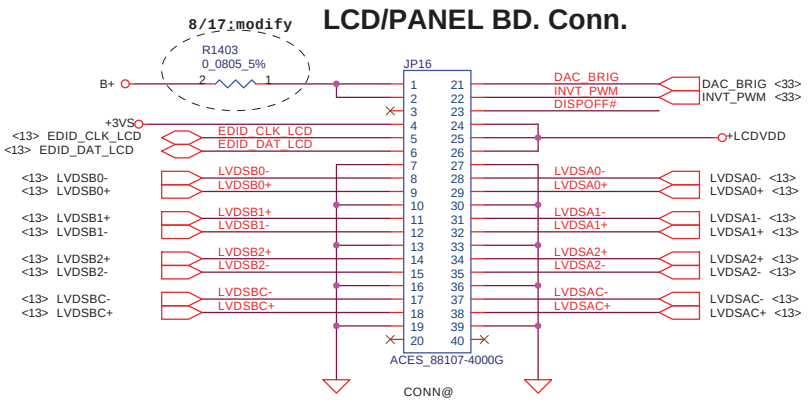
LCD POWER CIRCUIT





Security Classification	Compal Secret Data		
Issued Date	2005/03/01	Deciphered Date	2005/04/06

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Title	LCD Conn		
Size: Custom	Document Number: LA-2931		Rev: 0.3
Date: Thursday, August 18, 2005	Sheet 17 of 48		

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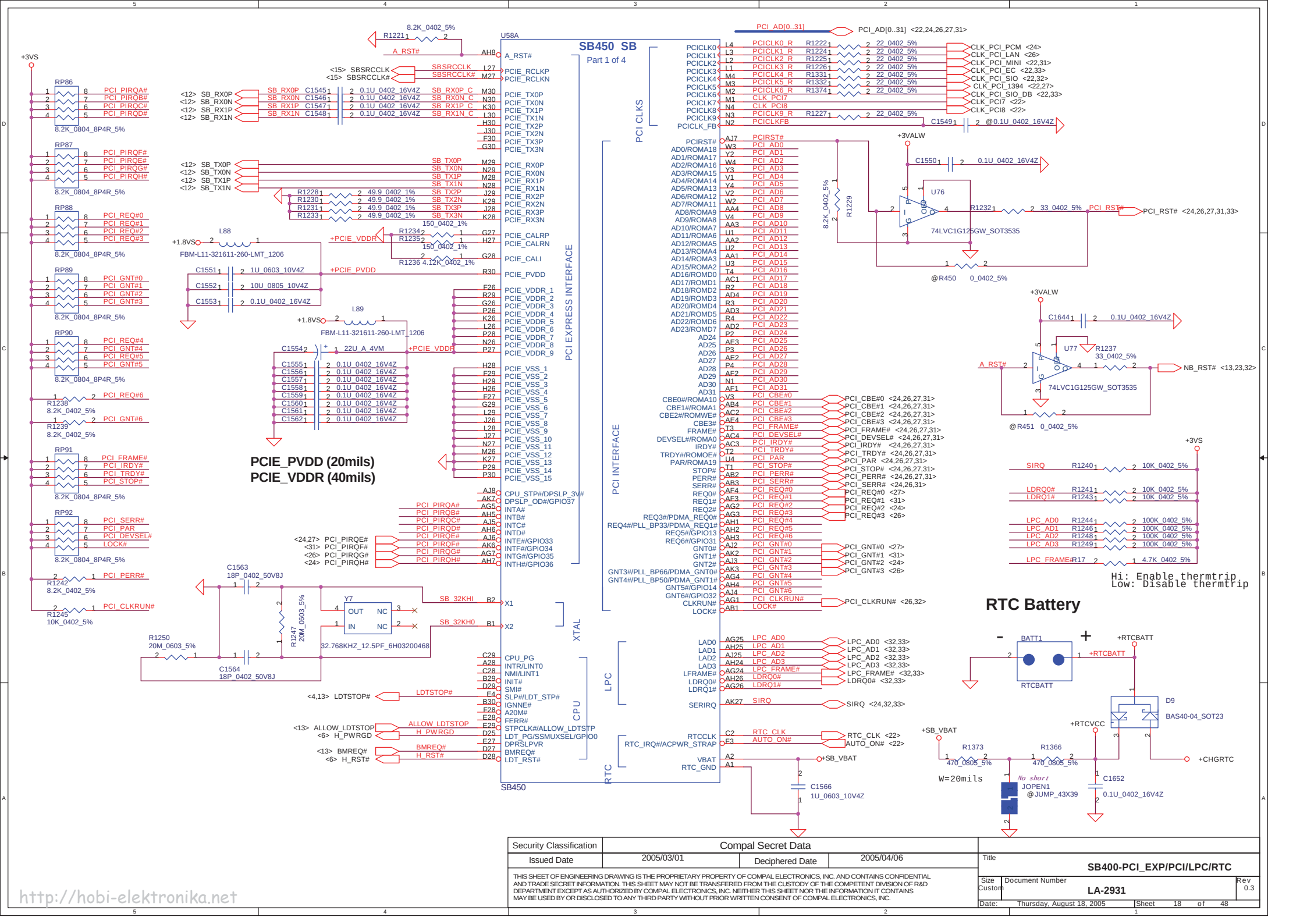
SB450 SB
Part 1 of 4
U58A
SB450
PCIE_PVDD (20mils)
PCIE_VDDR (40mils)
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
XTAL
LPC
CPU
RTC
RTC Battery
Hi: Enable thermtrip
Low: Disable thermtrip
W=20mils
No short
JOPEN1
@JUMP_43X39
74LVC1G125GW_SOT3535
FBM-L11-321611-260-LMT_1206
32.768KHZ_12.5PF_6H03200468
BAS40-04_SOT23
Security Classification
Compal Secret Data
Issued Date
2005/03/01
Deciphered Date
2005/04/06
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Title
SB400-PCI_EXP/PCI/LPC/RTC
Size
Custom
Document Number
LA-2931
Rev
0.3
Date:
Thursday, August 18, 2005
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18
of
48
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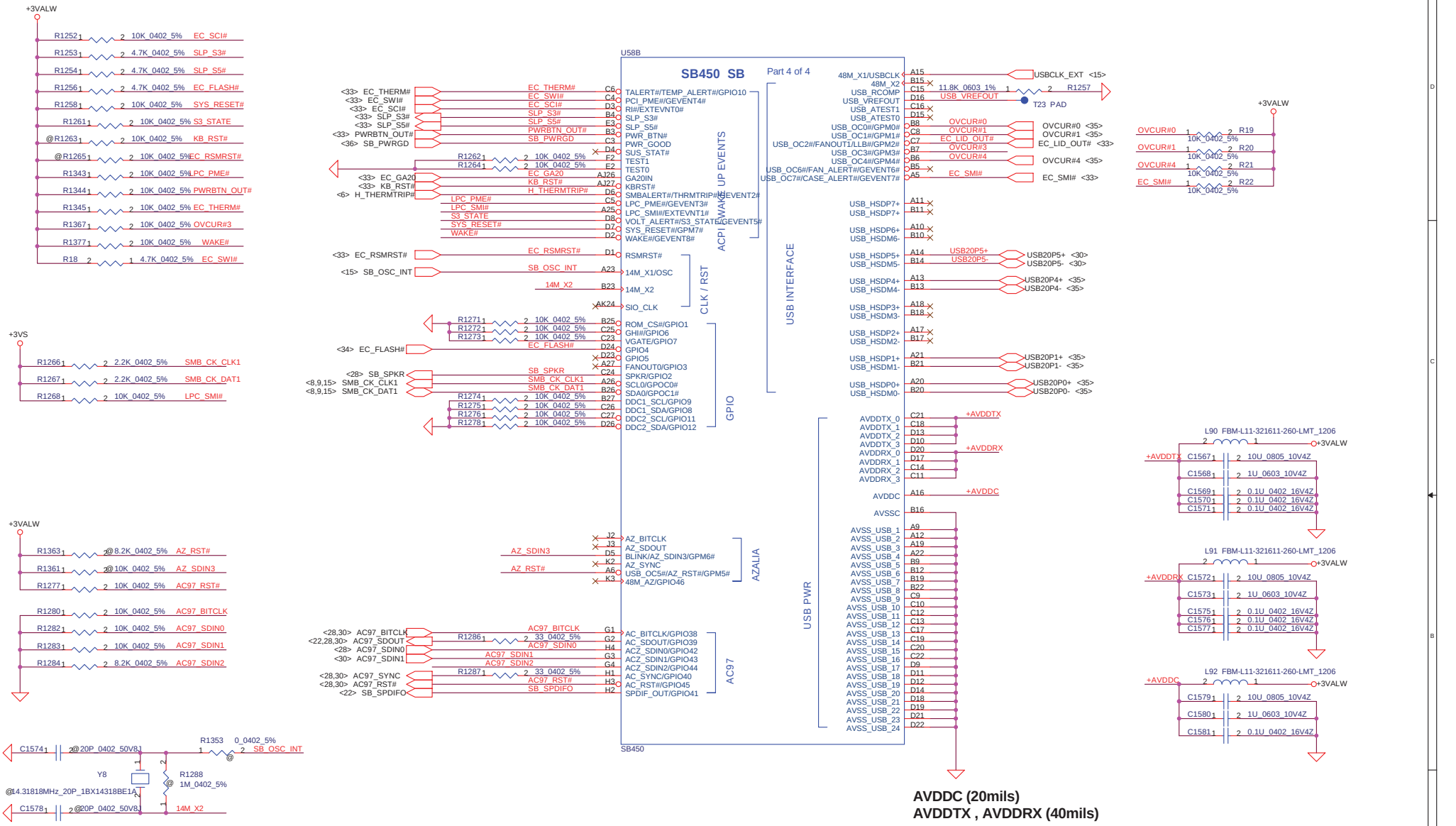

	GPIO12	GPIO11
HYNIX 128MB	0	1
SAMSUMG 128MB	1	1
* No VRAM	0	0
Reserved	1	0

AVDDC (20mils)
AVDDTX , AVDDRX (40mils)

Security Classification	Compal Secret Data		
Issued Date	2005/03/01	Deciphered Date	2005/04/06

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Title	SB400-USB/ACPI/AC97/GPIO		
Size Custom	Document Number LA-2931		Rev 0.3
Date: Thursday, August 18, 2005	Sheet 19 of 48		

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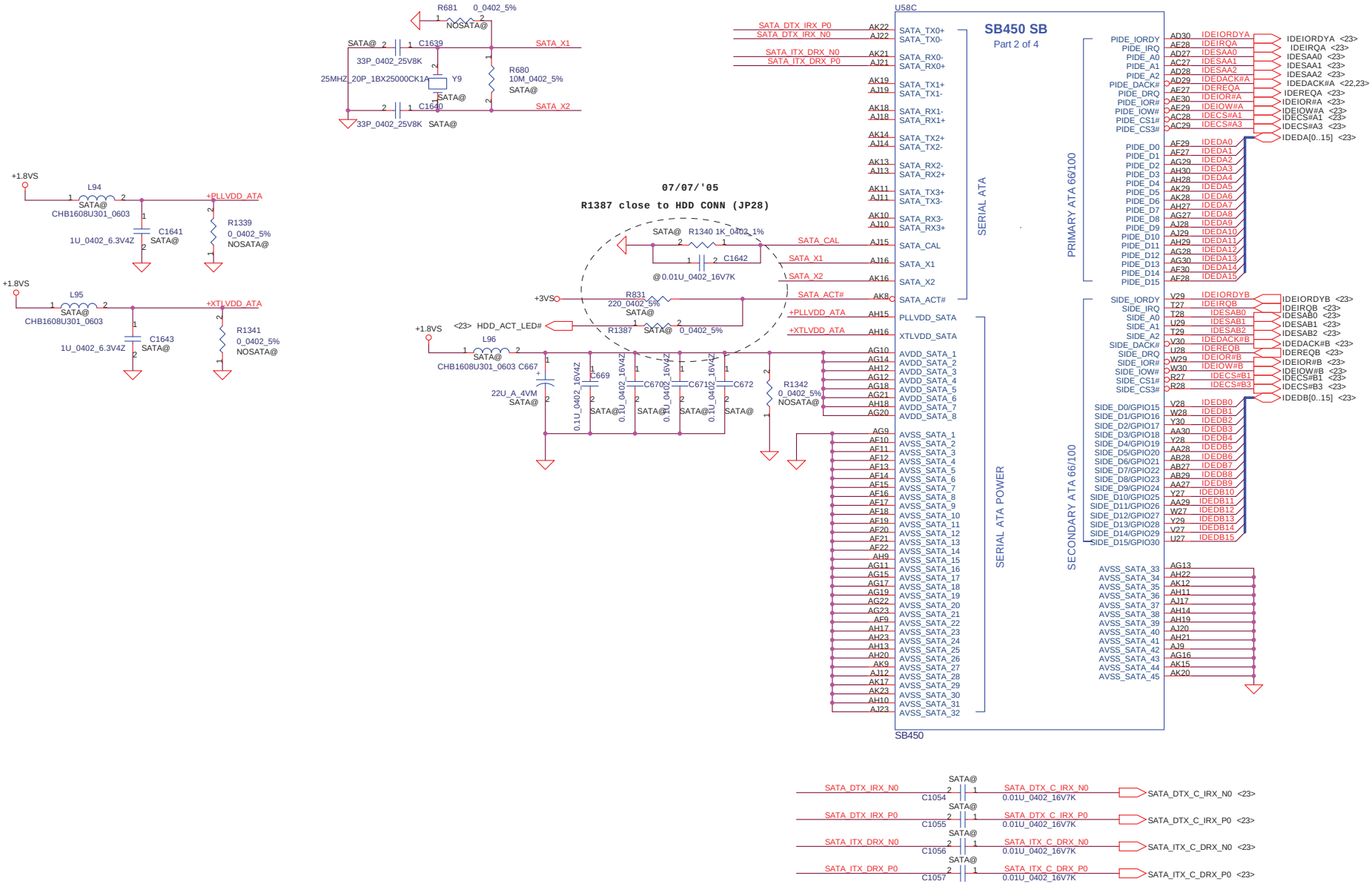

Security Classification	Compal Secret Data		
Issued Date	2005/03/01	Deciphered Date	2005/04/06

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Title	SB400-IDE/SATA		
Size: Custom	Document Number: LA-2931		Rev: 0.3
Date: Thursday, August 18, 2005	Sheet 20 of 48		

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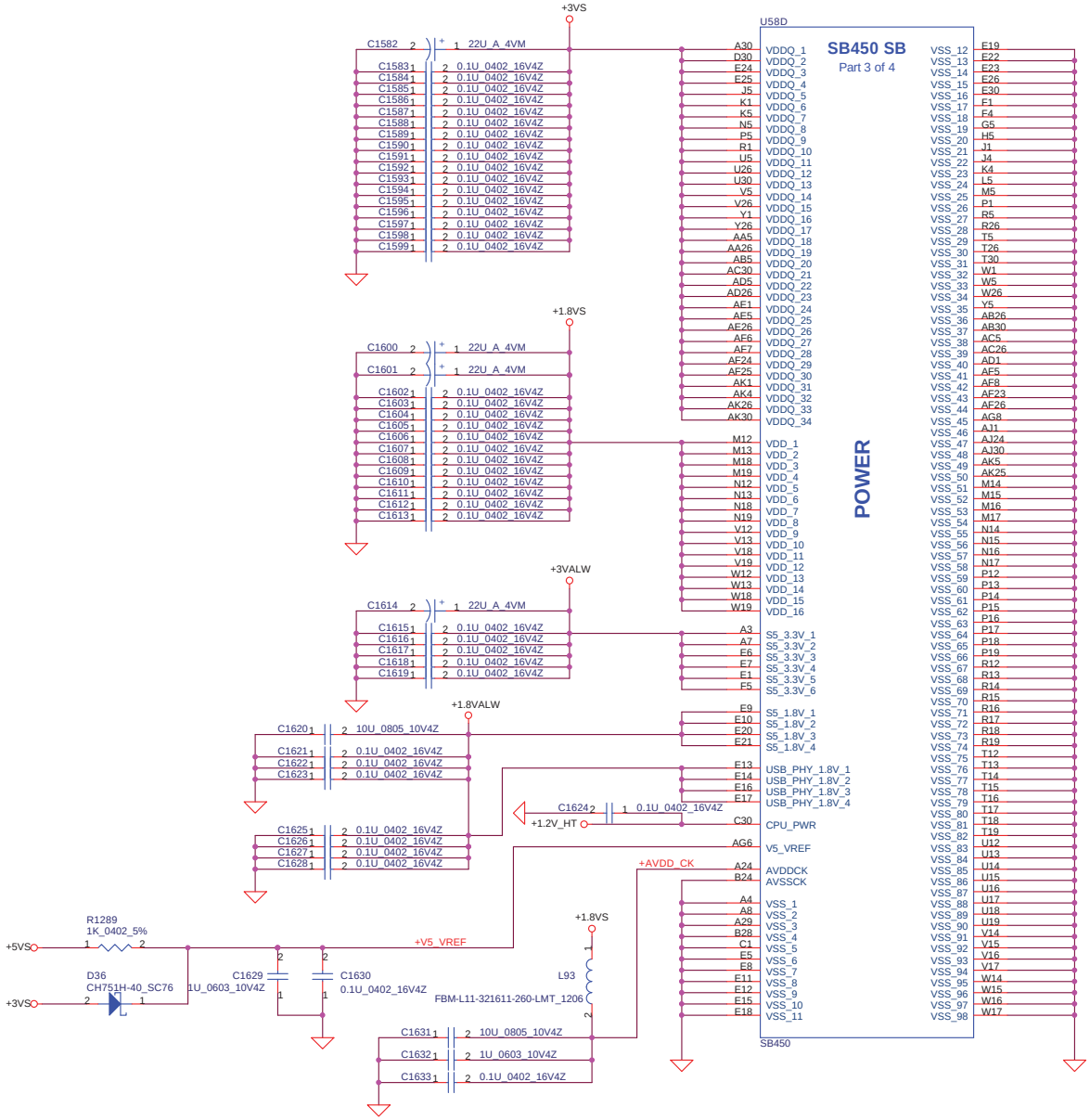

V5_VREF (20mils)
AVDD_CK(40mils)

Security Classification	Compal Secret Data		
Issued Date	2005/03/01	Deciphered Date	2005/04/06

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Title: **SB400-Power/GND**

Size	Document Number	Rev
Custom	LA-2931	0.3

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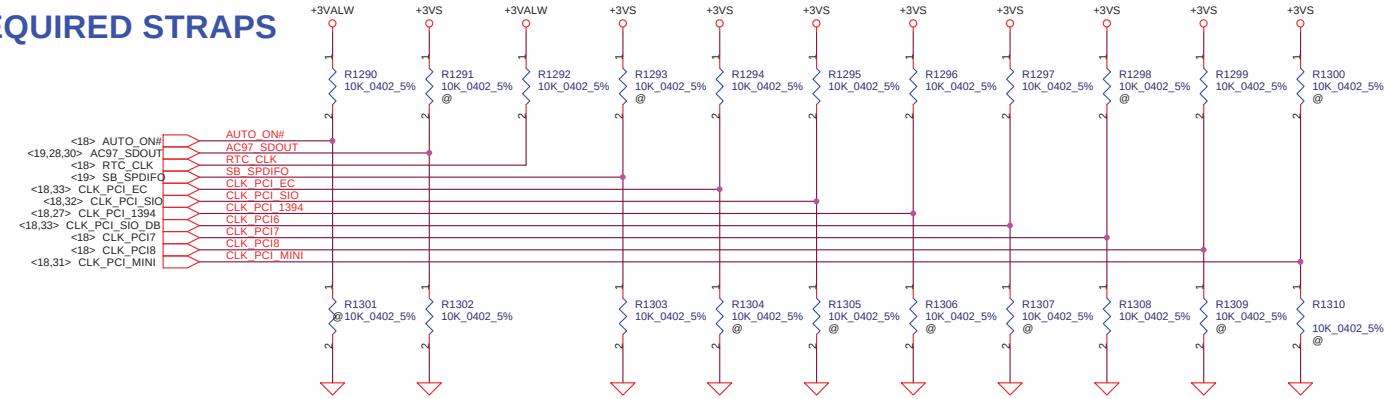
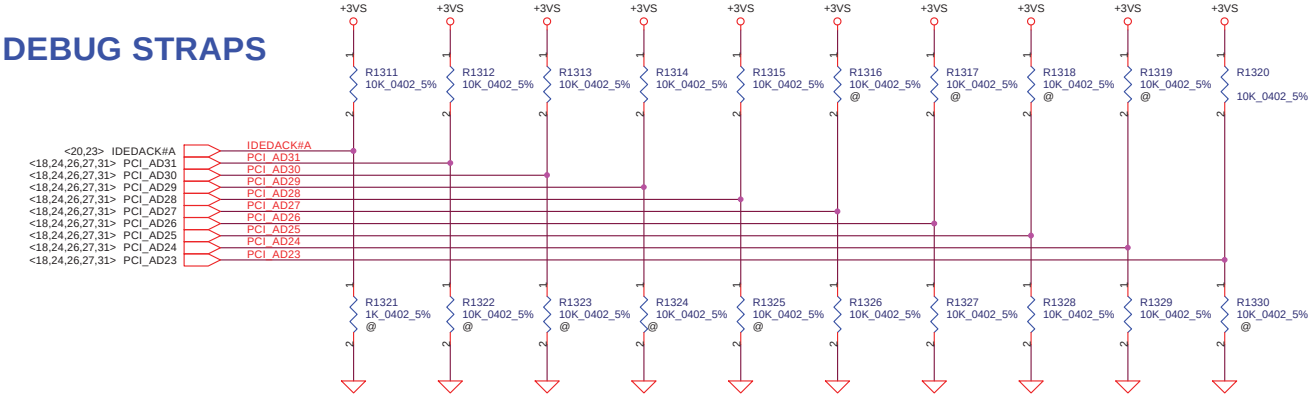
REQUIRED STRAPS



ACPWRON

	AUTO_ON#	AC97_SDOUT	RTC_CLK	SB_SPDIFO	CLK_PCI_MINI	CLK_PCI_EC	CLK_PCI_SIO	CLK_PCI_1394	PCI_CLK2 / CPU I/F	PCI_CLK3 / CLK_PCI7 / PCI_CLK4 / PCI_CLK5 / CLK_PCI6 / PCI_CLK8
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz OSC MODE	USB PHY PWRDOWN DISABLE DEFAULT	INTERNAL 48MHz DEFAULT	PCIE_CM_SET LOW DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM L,H = NORMAL LPC ROM DEFAULT L,L = FWH ROM
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	48MHz XTAL MODE	USB PHY PWRDOWN ENABLE	EXTERNAL 48MHz	PCIE_CM_SET High	CPU I/F = P4	

DEBUG STRAPS



	PD_DACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

Security Classification	Compal Secret Data		
Issued Date	2005/03/01	Deciphered Date	2005/04/06

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Title	Hardware Trap		
Size: Custom	Document Number: LA-2931		Rev: 0.3
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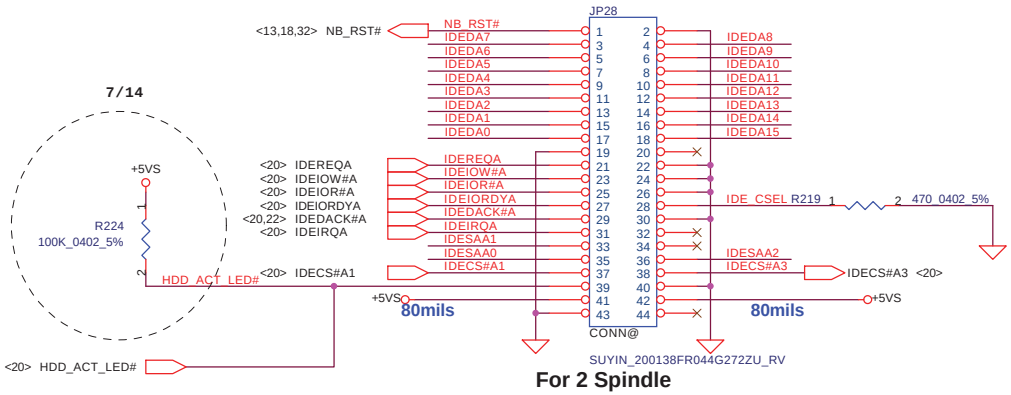
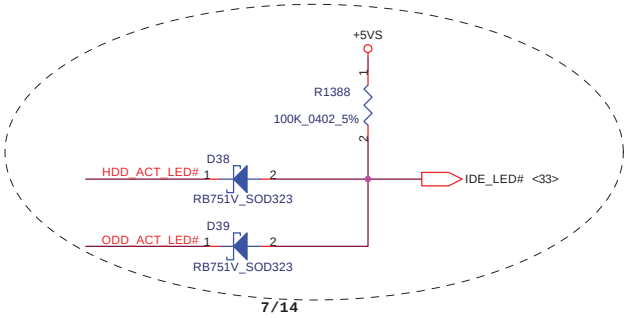
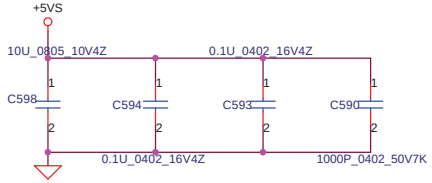
HDD CONN

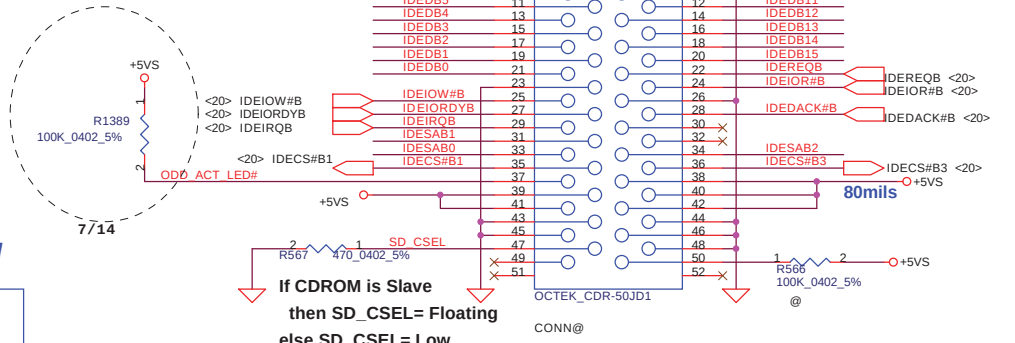


For 2 Spindle

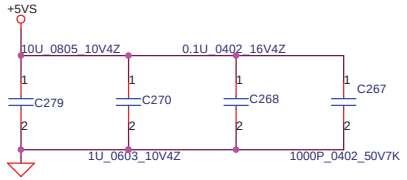


CDROM CONN

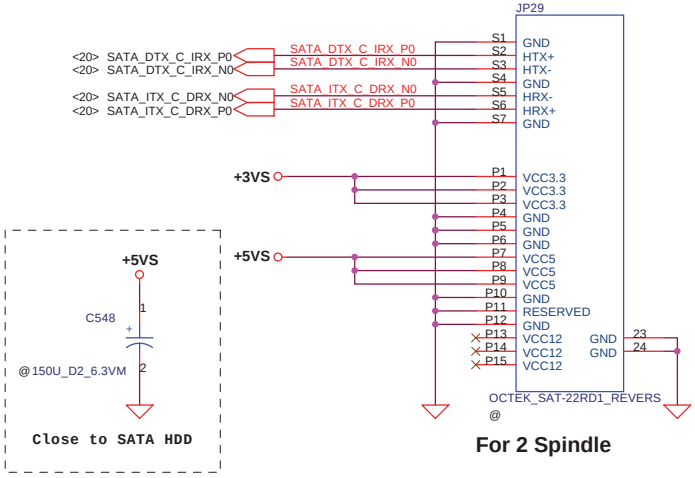




If CDROM is Slave
then SD_CSEL= Floating
else SD_CSEL= Low



SATA HDD CONN



For 2 Spindle

Security Classification	Compal Secret Data		
Issued Date	2005/03/01	Deciphered Date	2005/04/06

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Title	HDD/CDROM		
Size: Custom	Document Number: LA-2931		Rev: 0.3
Date: Thursday, August 18, 2005	Sheet 23 of 48		

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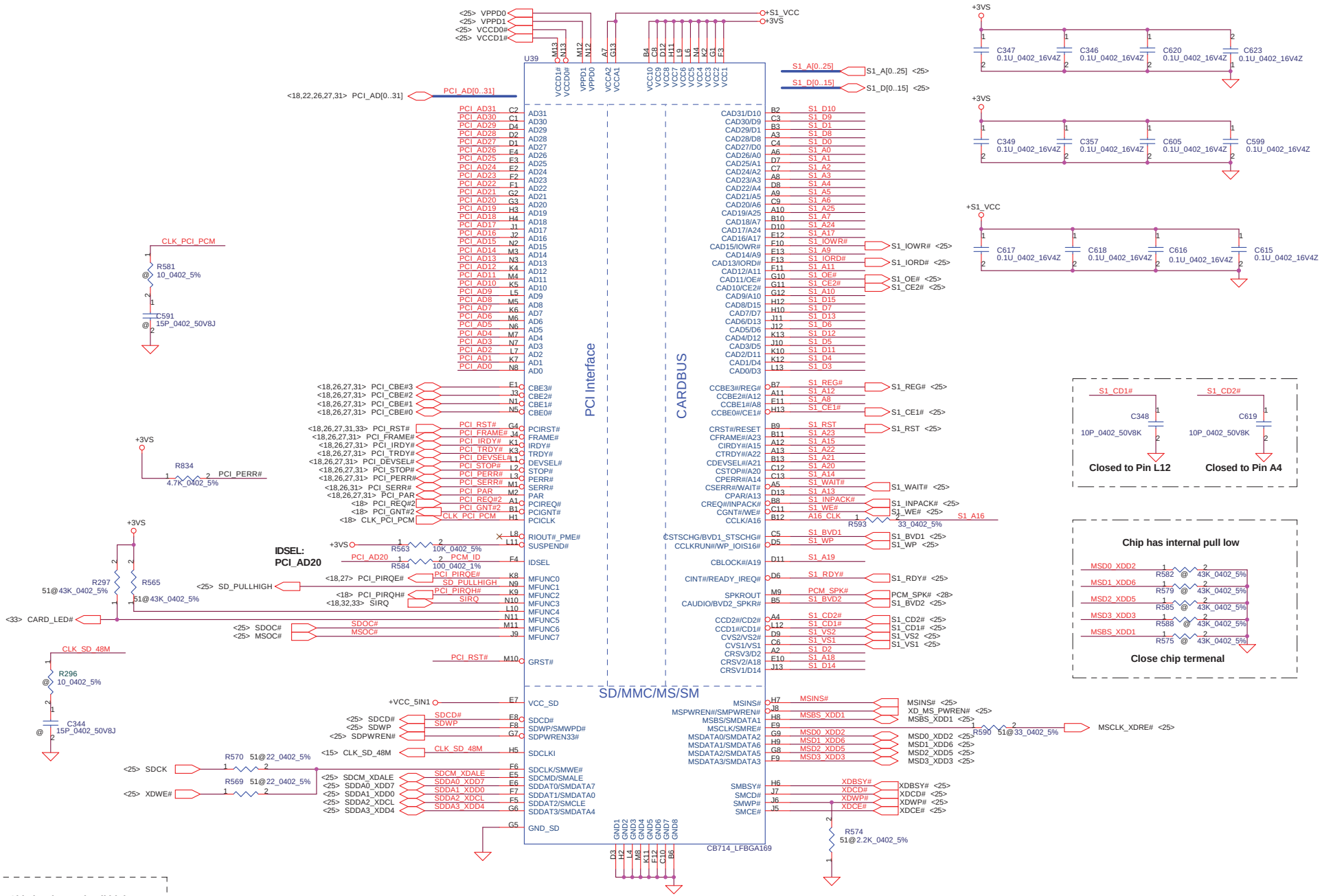

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Title	PCMCIA ENE CB714		
Size: Custom	Document Number: LA-2931		Rev: 0.3
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PCMCIA Power Controller

Don't support 12V card

U36 — CP2211D3_SSOP16

+S1_VCC 40mil: C585 0.1U_0402_16V4Z, C584 0.1U_0402_16V4Z, C586 10U_0805_10V4Z

+S1_VPP 20mil: C583 0.01U_0402_16V7K, C587 1U_0603_10V4Z

+5VS: C573 0.1U_0402_16V4Z, C570 4.7U_0805_10V4Z

+3VS: C574 0.1U_0402_16V4Z, C571 4.7U_0805_10V4Z

R562 10K_0402_5%

VCCD0# <24>, VCCD1# <24>, VPPD0 <24>, VPPD1 <24>

R550 @ 0_0805_5%

Reserve for SD pull high issue.

Chip has internal pull high

Close to CardBus Conn.

+S1_VCC: C337 10U_0805_10V4Z, C339 0.1U_0402_16V4Z

+S1_VPP: C343 4.7U_0805_10V4Z, C341 0.01U_0402_16V7K

SD/ MMC/ MS

R552 @43K_0402_5% — <24> XDCD# — XD_CD#

Q45 2N7002_SOT23 — MSINS#

51@

SDDA3_XDD4 <24>
SDDA1_XDD0 <24>
SDDA0_XDD7 <24>
SDCM_XDALE <24>
SDDA2_XDCL <24>
MSBS_XDD1 <24>
MSD1_XDD6 <24>
MSD0_XDD2 <24>
MSD2_XDD5 <24>
MSINS# <24>
MSD3_XDD3 <24>
SDWP <24>
SDCD# <24>

+VCC_5IN1: C589 @1U_0603_10V4Z, C580 51@0.1U_0402_16V4Z, C588 51@0.1U_0402_16V4Z

+VCC_SM/XD

XDBSY# <24> — R551 51@43K_0402_5%

XDCE# <24> — R547 51@43K_0402_5%

MSCLK_XDRE# — R564 51@43K_0402_5%

XDWE# <24> — R545 51@2.2K_0402_5%

SD CLK

<24> SDCK — SDCK — C579 @10P_0402_50V8K

MS CLK

<24> MSCLK_XDRE# — MSCLK_XDRE# — R549 @0_0402_5% — C572 @10P_0402_50V8K

+SD_PULLHIGH by BIOS setting

<24> SD_PULLHIGH — SD_PULLHIGH

R294 @ 43K_0402_5% SD_PULLHIGH
R557 @ 43K_0402_5% SDCM_XDALE
R553 @ 43K_0402_5% SDDA0_XDD7
R541 @ 43K_0402_5% SDDA1_XDD0
R560 @ 43K_0402_5% SDDA2_XDCL
R559 @ 43K_0402_5% SDDA3_XDD4

Close to 5 in 1 socket

JP36 — 4 IN 1 CONN — SD / MMC / MS(PRO) / XD — 51@TAITW_R007-520-L3

+VCC_5IN1 → XD-VCC, SD-VCC, MS-VCC

SDDA1_XDD0 → XD-D0
MSBS_XDD1 → XD-D1
MSD0_XDD2 → XD-D2
MSD3_XDD3 → XD-D3
SDDA3_XDD4 → XD-D4
MSD2_XDD5 → XD-D5
MSD1_XDD6 → XD-D6
SDDA0_XDD7 → XD-D7

SD-CLK → SDCK
SD-DAT0 → SDDA0_XDD7
SD-DAT1 → SDDA1_XDD0
SD-DAT2 → SDDA2_XDCL
SD-DAT3 → SDDA3_XDD4
SD-CMD → SDCM_XDALE
SD-CD-SW → SDCD#
SD-WP-SW → SDWP

<24> XDWP# → XDWE#, XDWP#, SDCM_XDALE, XD_CD#, XDBSY#, MSCLK_XDRE#, XDCE#, SDDA2_XDCL → XD-WE, XD-WP, XD-ALE, XD-CD, XD-R/B, XD-RE, XD-CE, XD-CLE

MS-SCLK → MSCLK_XDRE#
MS-DATA0 → MSD0_XDD2
MS-DATA1 → MSD1_XDD6
MS-DATA2 → MSD2_XDD5
MS-DATA3 → MSD3_XDD3
MS-INS → MSINS#
MS-BS → MSBS_XDD1

GND, GND → 4IN1-GND, 4IN1-GND

+VCC_SM/XD: C656 @1U_0603_10V4Z, C657 51@0.1U_0402_16V4Z

+VCC_5IN1: C551 @1U_0603_10V4Z, C556, C555, C554, C553 — 51@0.1U_0402_16V4Z

CardBus Socket

JP7 — SANTA_130609-1_LT — CONN@

S1_A[0..25], S1_D[0..15]

GND, GND, DATA3, CD1#, DATA4, DATA11, DATA5, DATA12, DATA6, DATA13, DATA7, DATA14, CE1#, DATA15, ADD10, CE2#, OE#, VS1#, ADD11, IORD#, ADD9, IOWR#, ADD8, ADD17, ADD13, ADD18, ADD14, ADD19, WE#, ADD20, READY, ADD21, VCC, VCC, VPP, VPP, ADD16, ADD22, ADD15, ADD23, ADD12, ADD24, ADD7, ADD25, ADD6, VS2#, ADD5, RESET, ADD4, WAIT#, ADD3, INPACK#, ADD2, REG#, ADD1, BVD2, ADD0, BVD1, DATA0, DATA8, DATA1, DATA9, DATA2, DATA10, WP, CD2#, GND, GND, GND, GND

S1_D3, S1_CD1#, S1_D4, S1_D11, S1_D5, S1_D12, S1_D6, S1_D13, S1_D7, S1_D14, S1_CE1#, S1_D15, S1_A10, S1_CE2#, S1_OE#, S1_VS1, S1_A11, S1_IORD#, S1_A9, S1_IOWR#, S1_A8, S1_A17, S1_A13, S1_A18, S1_A14, S1_A19, S1_WE#, S1_A20, S1_RDY#, S1_A21, +S1_VCC, +S1_VCC, +S1_VPP, +S1_VPP, S1_A16, S1_A22, S1_A15, S1_A23, S1_A12, S1_A24, S1_A7, S1_A25, S1_A6, S1_VS2, S1_A5, S1_RST, S1_A4, S1_WAIT#, S1_A3, S1_INPACK#, S1_A2, S1_REG#, S1_A1, S1_BVD2, S1_A0, S1_BVD1, S1_D0, S1_D8, S1_D1, S1_D9, S1_D2, S1_D10, S1_WP, S1_CD2#

<24> S1_CD1#, <24> S1_CE1#, <24> S1_CE2#, <24> S1_OE#, <24> S1_VS1, <24> S1_IORD#, <24> S1_IOWR#, <24> S1_WE#, <24> S1_RDY#, <24> S1_VS2, <24> S1_RST, <24> S1_WAIT#, <24> S1_INPACK#, <24> S1_REG#, <24> S1_BVD2, <24> S1_BVD1, <24> S1_WP, <24> S1_CD2#

5 IN 1 PWR Control

U49 — 51@TPS2041ADR_SO8

+3VS, +VCC_5IN1

R536 51@4.7K_0402_5%

<24> SDPWREN#

<24> XD_MS_PWREN# — R632 51@0_0402_5%

R531 51@100K_0402_5%

R537 51@10K_0402_5%

R538 51@0_0402_5% — SDOC# <24>

R633 51@0_0402_5% — MSOC# — MSOC# <24>

R571 51@0_0603_5% — +VCC_5IN1 → +VCC_SM/XD

5 IN 1 PWR Control

U48 — @RT9702ACB_SOT23-5

R627 @10K_0402_5%

R629 @4.7K_0402_5%

Q44 @DTC115EKA_SOT23 — XD_MS_PWREN#

R628 @0_0402_5%

R630 @100K_0402_5%

R626 @10K_0402_5%

C666 @0.1U_0402_16V4Z

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Title: PCMCIA Socket

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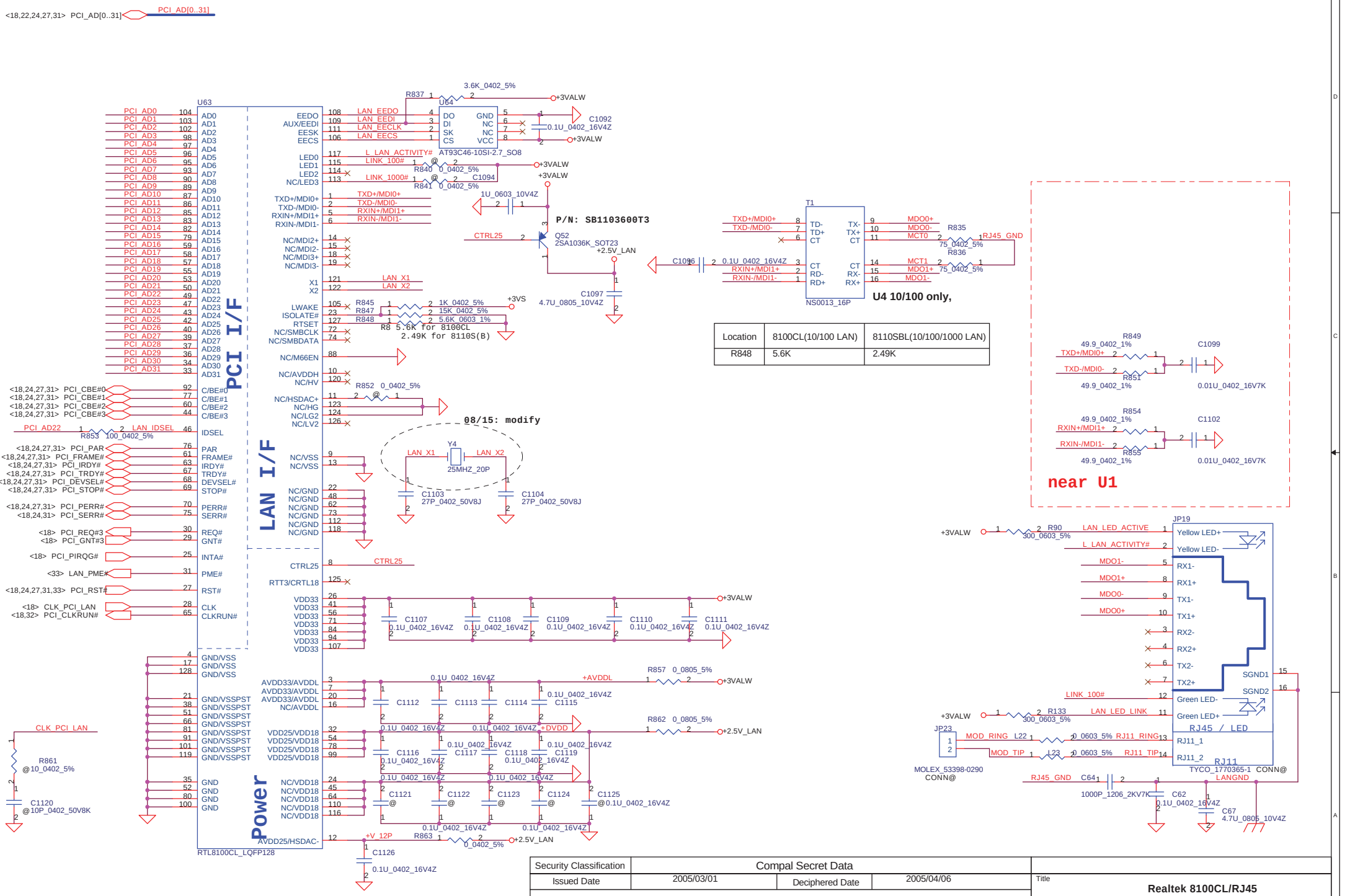

Location	8100CL(10/100 LAN)	8110SBL(10/100/1000 LAN)
R848	5.6K	2.49K

Security Classification	Compal Secret Data		
Issued Date	2005/03/01	Deciphered Date	2005/04/06

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Title	Realtek 8100CL/RJ45		
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Analog Pin		
Pin	VT6308S	VT6311S
74	XTPB1M	NC
75	XTPB1P	NC
76	XTPA1M	NC
77	XTPA1P	NC
78	XTPBIAS1	NC

VT6311S

PCI I/F

EEPROM

others

OSCILLATOR

PHY PORT0

PHY PORT1

U37

VT6311S_LQFP128

IDSEL:PCI_AD16

PCI_AD16 R533 1394_IDSEL 100_0402_5%

<18,22,24,26,31> PCI_AD[0..31]

PCI_AD31 94
PCI_AD30 95
PCI_AD29 96
PCI_AD28 97
PCI_AD27 98
PCI_AD26 101
PCI_AD25 102
PCI_AD24 103
PCI_AD23 106
PCI_AD22 107
PCI_AD21 109
PCI_AD20 113
PCI_AD19 114
PCI_AD18 115
PCI_AD17 116
PCI_AD16 117
PCI_AD15 2
PCI_AD14 3
PCI_AD13 4
PCI_AD12 7
PCI_AD11 8
PCI_AD10 9
PCI_AD9 10
PCI_AD8 11
PCI_AD7 14
PCI_AD6 15
PCI_AD5 16
PCI_AD4 18
PCI_AD3 19
PCI_AD2 20
PCI_AD1 24
PCI_AD0 25

<18,24,26,31> PCI_CBE#3 PCI_CBE#3 104
<18,24,26,31> PCI_CBE#2 PCI_CBE#2 119
<18,24,26,31> PCI_CBE#1 PCI_CBE#1 1
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<18,24,26,31> PCI_PERR# PCI_PERR# 127
<18,24,26,31> PCI_PAR PCI_PAR 128
<18,24> PCI_PIRQE# PCI_PIRQE# 88
<18,24,26,31,33> PCI_RST# PCI_RST# 89
<18,22> CLK_PCI_1394 CLK_PCI_1394 90
<18> PCI_GNT#0 PCI_GNT#0 92
<18> PCI_REQ#0 PCI_REQ#0 93
1394_IDSEL 105
<33> 1394_PME# 1394_PME# 34
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<18,24,26,31> PCI_TRDY# PCI_TRDY# 123
<18,24,26,31> PCI_DEVSEL# PCI_DEVSEL# 124
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+2.5VS_1394

+3VS

+1394_PLLVDD 0.01U_0402_16V7K L34 BLM21A601SPT_0805

C15 C12 C7 C569 C568 0.1U_0402_16V4Z 4.7U_0805_10V4Z

R554 I2CEEN 4.7K_0402_5%

U2 AT24C02N-10SI-2.7_SO8 A0 A1 A2 GND VCC WP SCL SDA EECK EEDI

R555 510_0402_5%

EECK and EEDI is pull high internal
External pull high circuit is unnecessary

R548 @ 4.7K_0402_5%

EEDI EECK

PHYRST# BJT_CTL I2CEN PWRDET REG_FB REG_OUT XCPS XREXT XI XO

6311@ R35 4.7K_0402_5%
R33 4.7K_0402_5%
C2 6301@ 1U_0402_6.3V4Z
C34 0.1U_0402_16V4Z
R372 1K_0402_5%
R362 6.19K_0603_1%
1394_X1 1394_X0
Q1 2SB1197K_SOT23 6311@
R38 6301@ 0_0603_5%
C575 C576 X2 10P_0402_50V8J
24.576MHz_16P_3XG-24576-43E1

XTPB0M XTPB0P XTPA0M XTPA0P XTPBIAS0 XTPB1M XTPB1P XTPA1M XTPA1P XTPBIAS1

NC17 NC16 NC15 NC14 NC13 NC12 NC11 NC10 NC9 NC8 NC7 NC6 NC5 NC4 NC3 NC2 NC1 NC0

R217 R218 C266 R220 R225 C271 R221
54.9_0402_1% 0.33U_0603_16V4Z 270P_0402_50V7K 4.99K_0402_1%

XTPBIAS0 XTPA0P XTPA0M XTPB0P XTPB0M

R1399 R1400 R1401 R1402 0_0402_5%
L100 L101 @WCM2012F2S-900T04_0805
XTPA0M_1 XTPA0P_1 XTPB0M_1 XTPB0P_1

JP30 GND1 GND2 GND3 GND4
CONN@ SUYIN_020204FR004S506ZL

Table 1

VT6311S VDD Power	BJT CTL Enable(R35)	VDD POWER (Q1)
Internal Regulator	REMOVE	REMOVE
External BJT	ON	ON

1394 CHIP	VCC/PWRDET Enable(R33)	VCC/PWRDET Enable(C2)	BJT CTL Enable(R35,Q1)	VCC/VDD POWER	XREXT (R36)
VT6301S	0 ohm	ON	REMOVE	R38 must mount. R39 doesn't mount.	6.34K 1%
VT6311S	4.7K ohm	REMOVE	ON See Table 1	R38 don't mount. R39 must mount. See Table 2	6.20K 1%

Table 2

Power Pin		
Pin	VT6301S	VT6311S
81	NC	BJT_CTL
84	NC	REG_FB
85	NC	REG_OUT
32	VCC(+3.3V)	PWRDET
36	PVD(+3.3V)	VCC(+3.3V)
46	PVD(+3.3V)	VDD(+2.5V)
21	VCC(+3.3V)	VDD(+2.5V)
111	VCC(+3.3V)	VDD(+2.5V)
30	VCC(+3.3V)	VDD(+2.5V)
PHY Differential Pin		
74	NC	NC
75	NC	NC
76	NC	NC
77	NC	NC
78	NC	NC

+2.5VS_1394 C17 C18 C19 C20 0.1U_0402_16V4Z

+3VS C22 C23 C24 C26 C31 C32 0.1U_0402_16V4Z

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Title: VIA 1394 VT6311S

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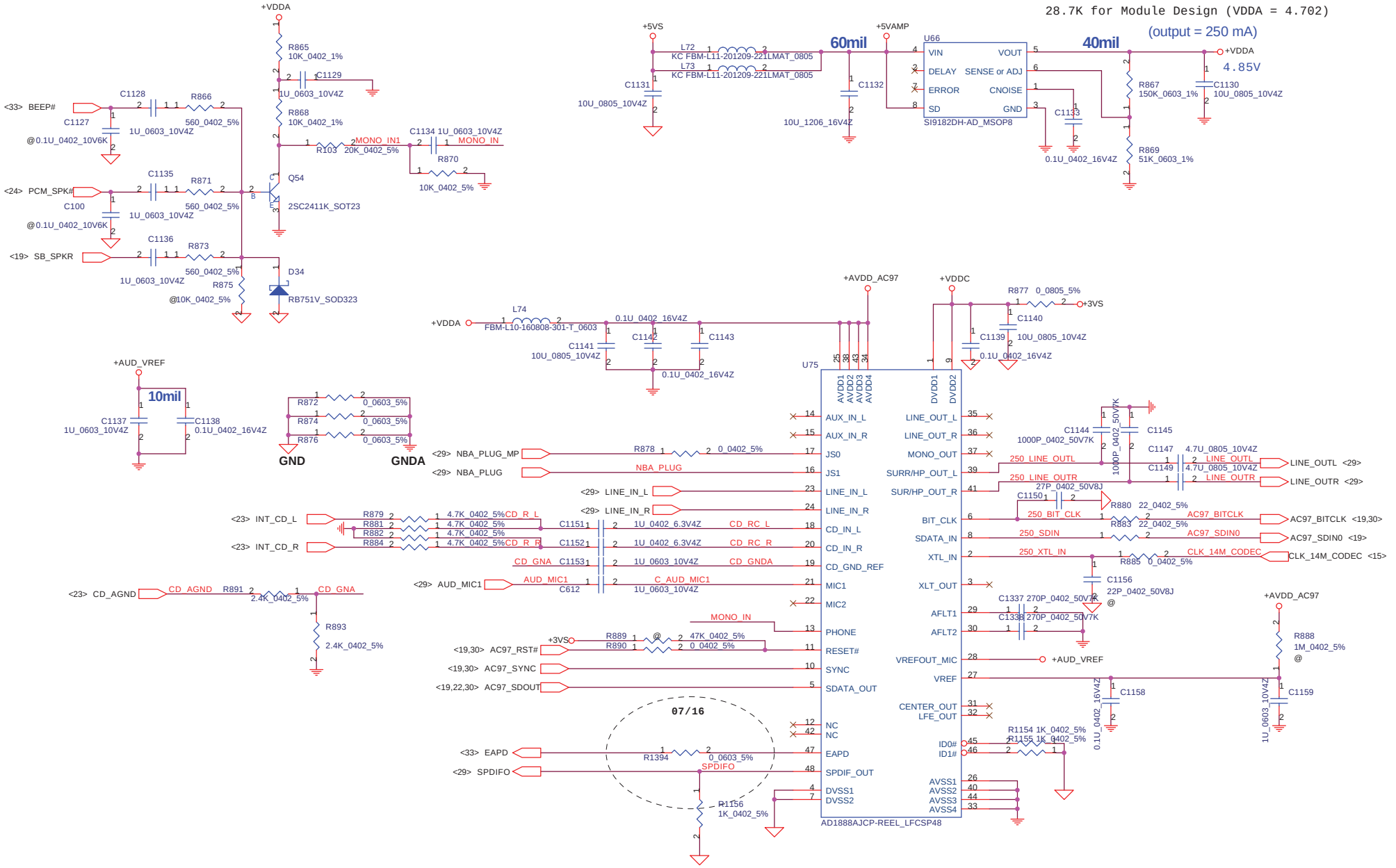
AC97 Codec

28.7K for Module Design (VDDA = 4.702)

(output = 250 mA)



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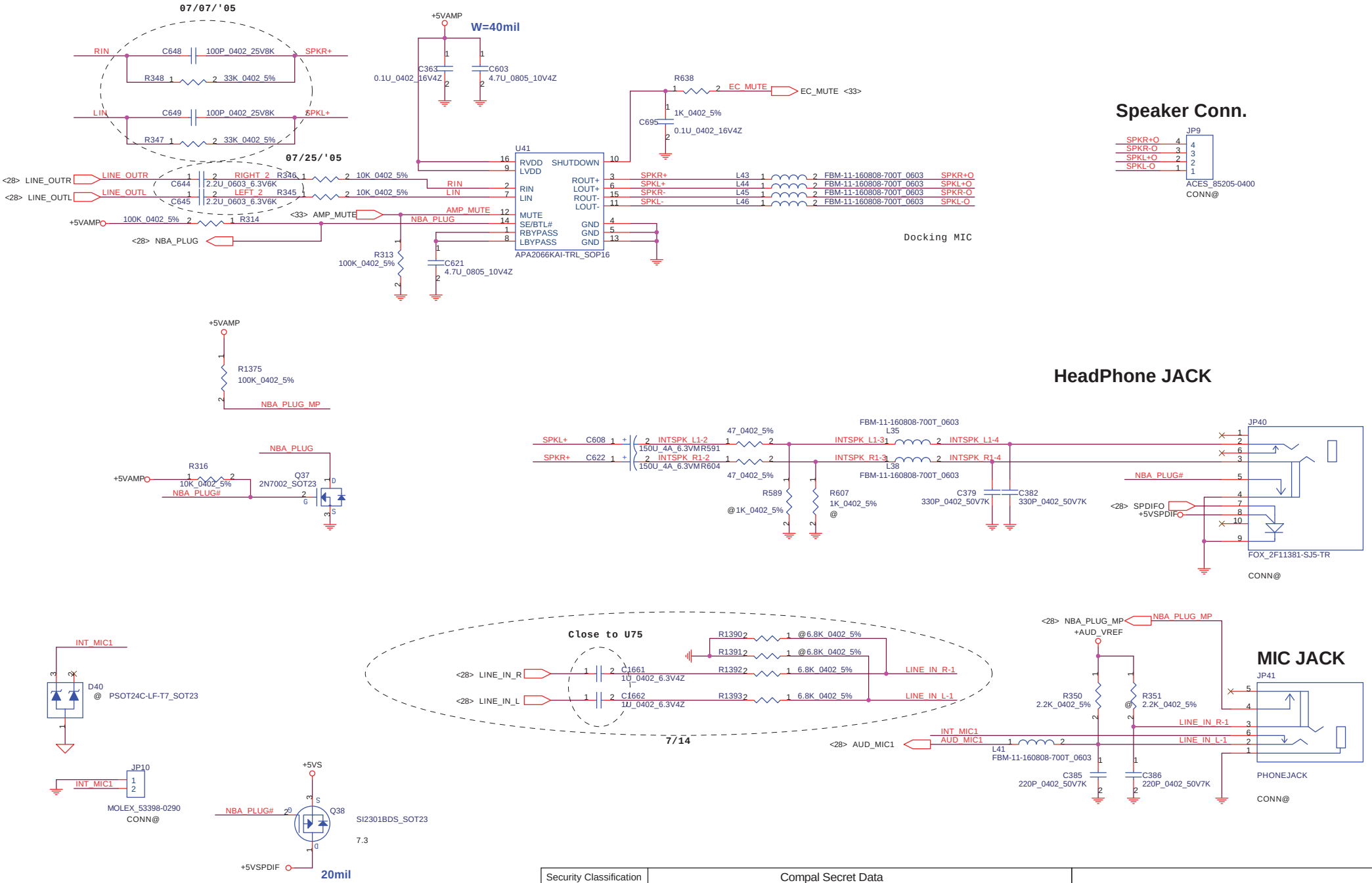

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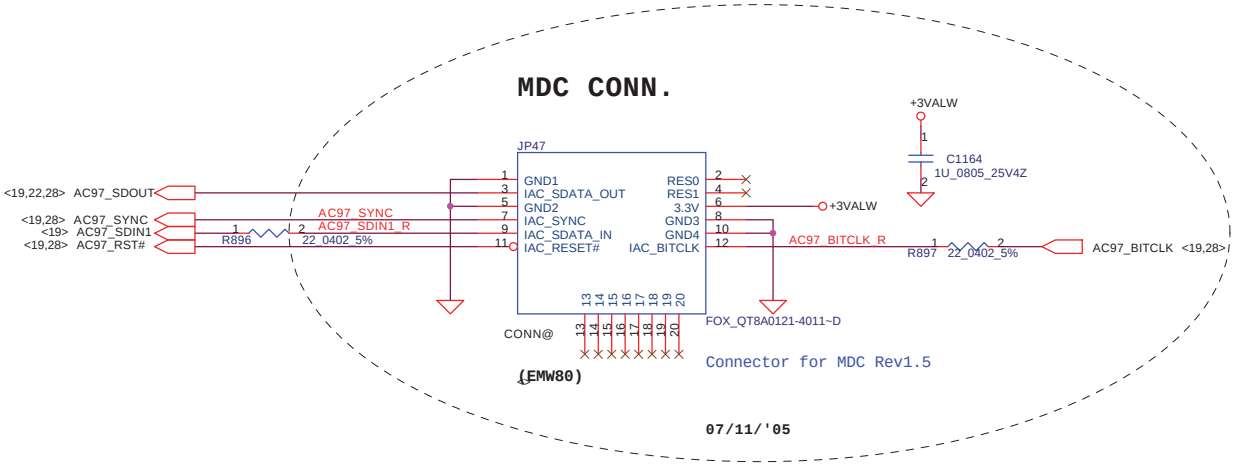
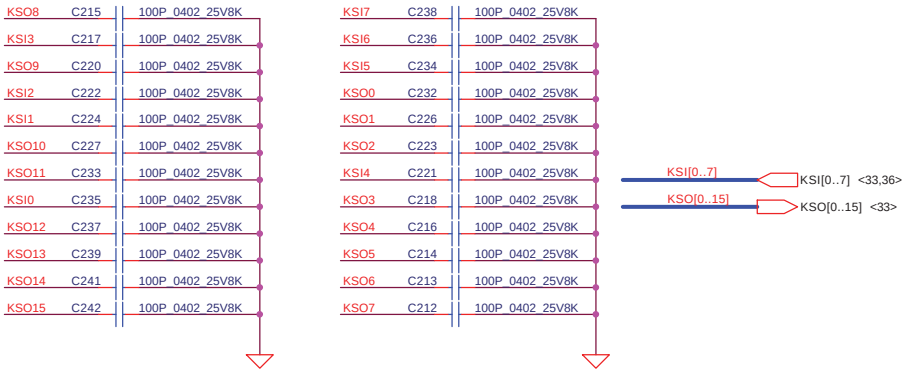
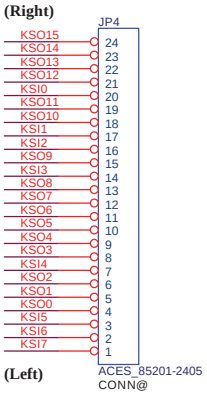
MDC CONN.

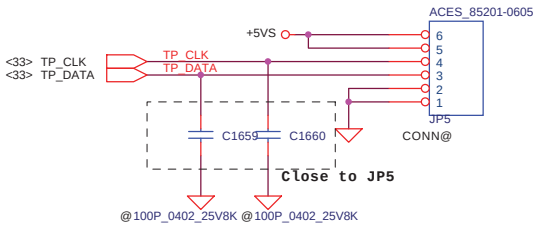




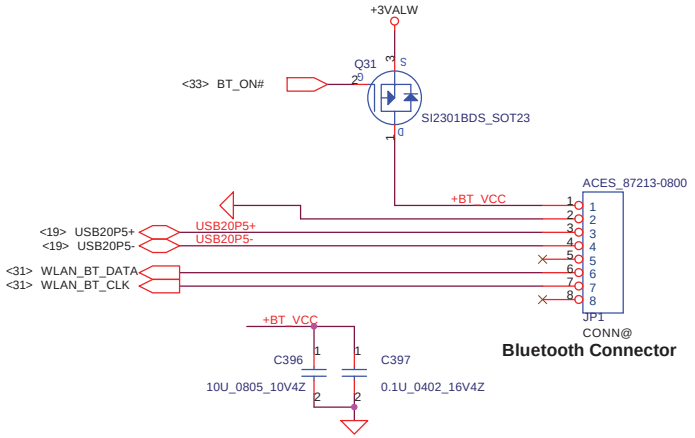
INT_KBD CONN.



TO M/B



BlueTooth Interface



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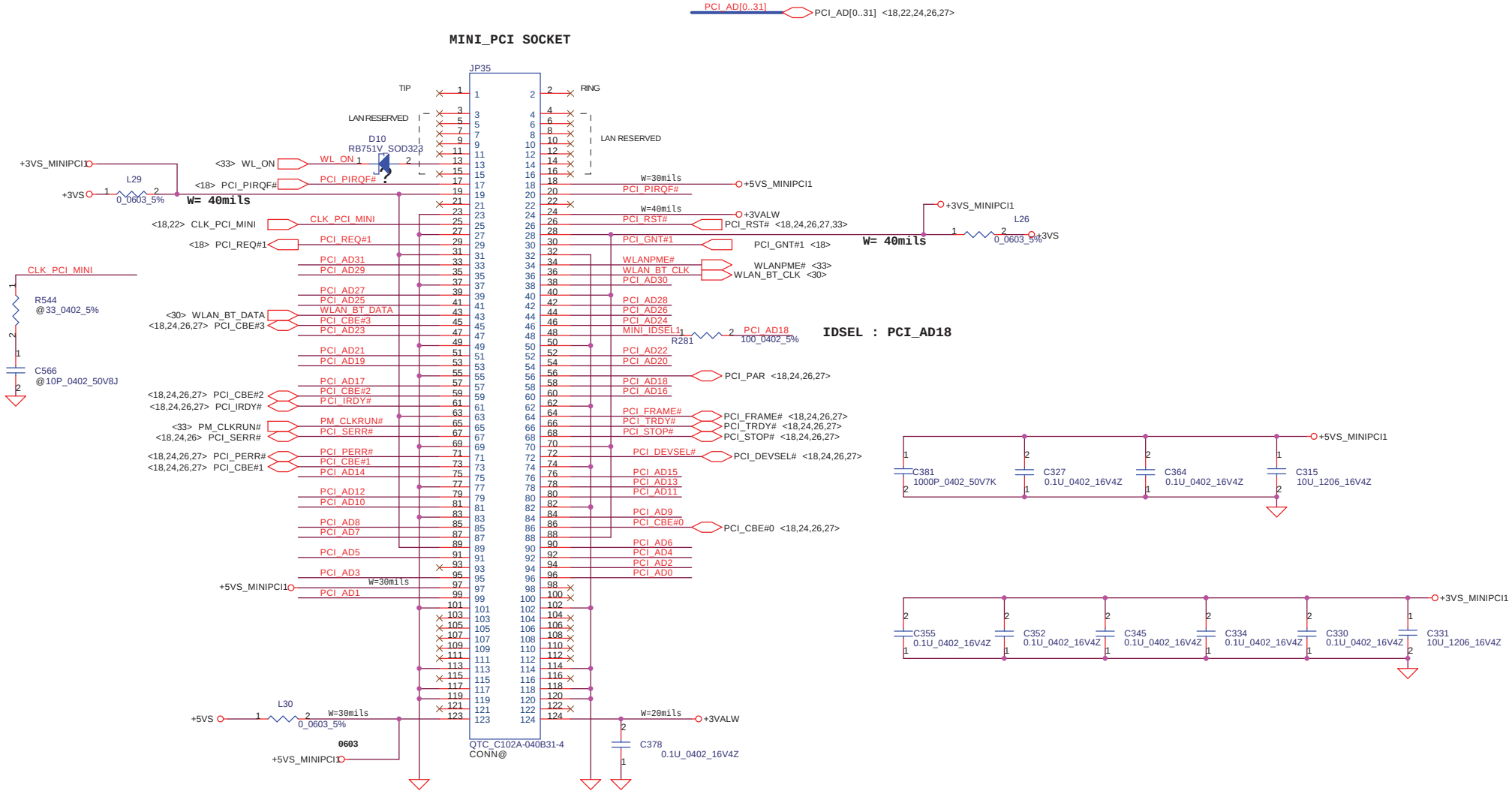

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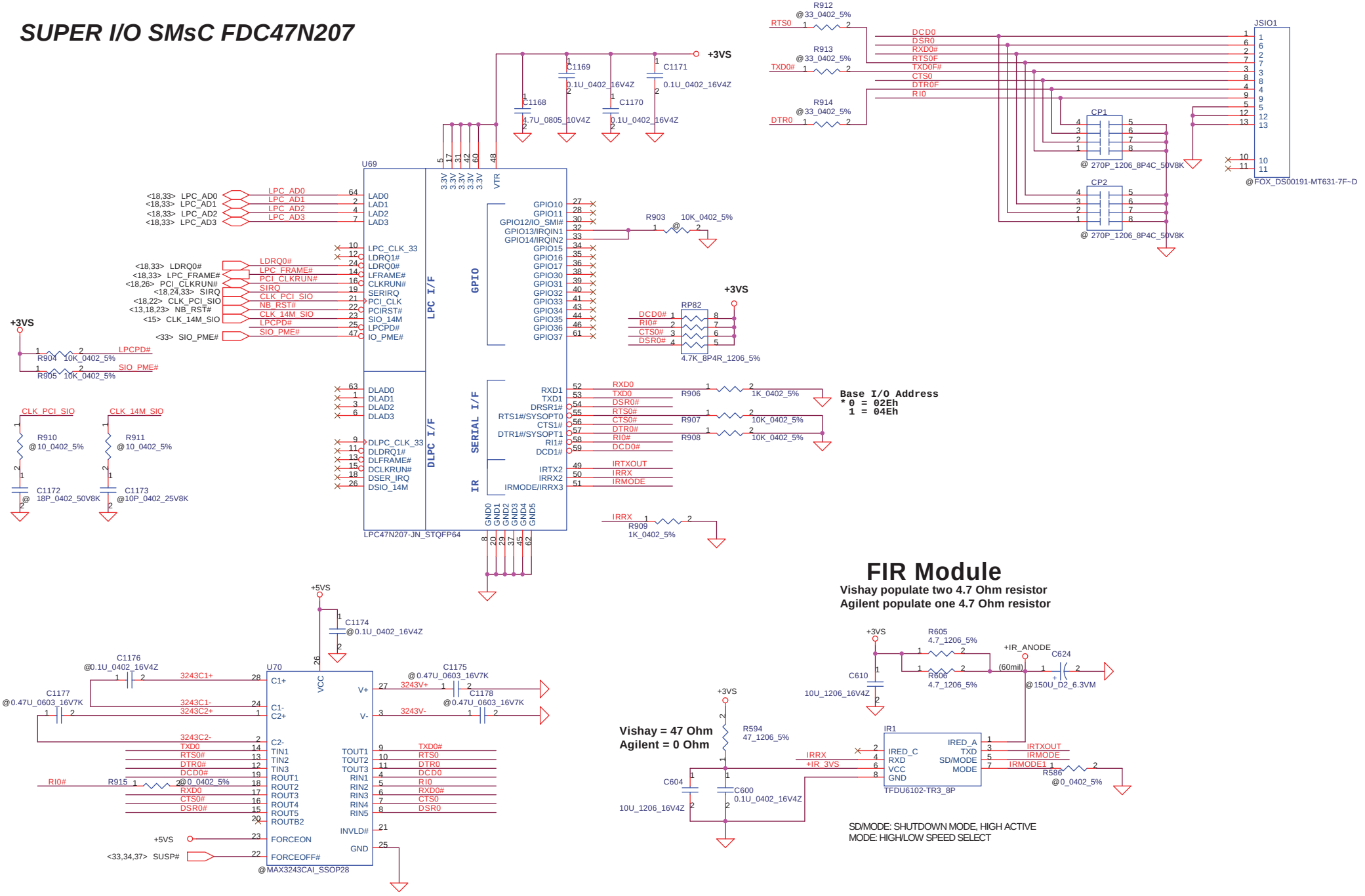
SUPER I/O SMsC FDC47N207



FIR Module

Vishay populate two 4.7 Ohm resistor
Agilent populate one 4.7 Ohm resistor

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Title	Super IO/FIR		
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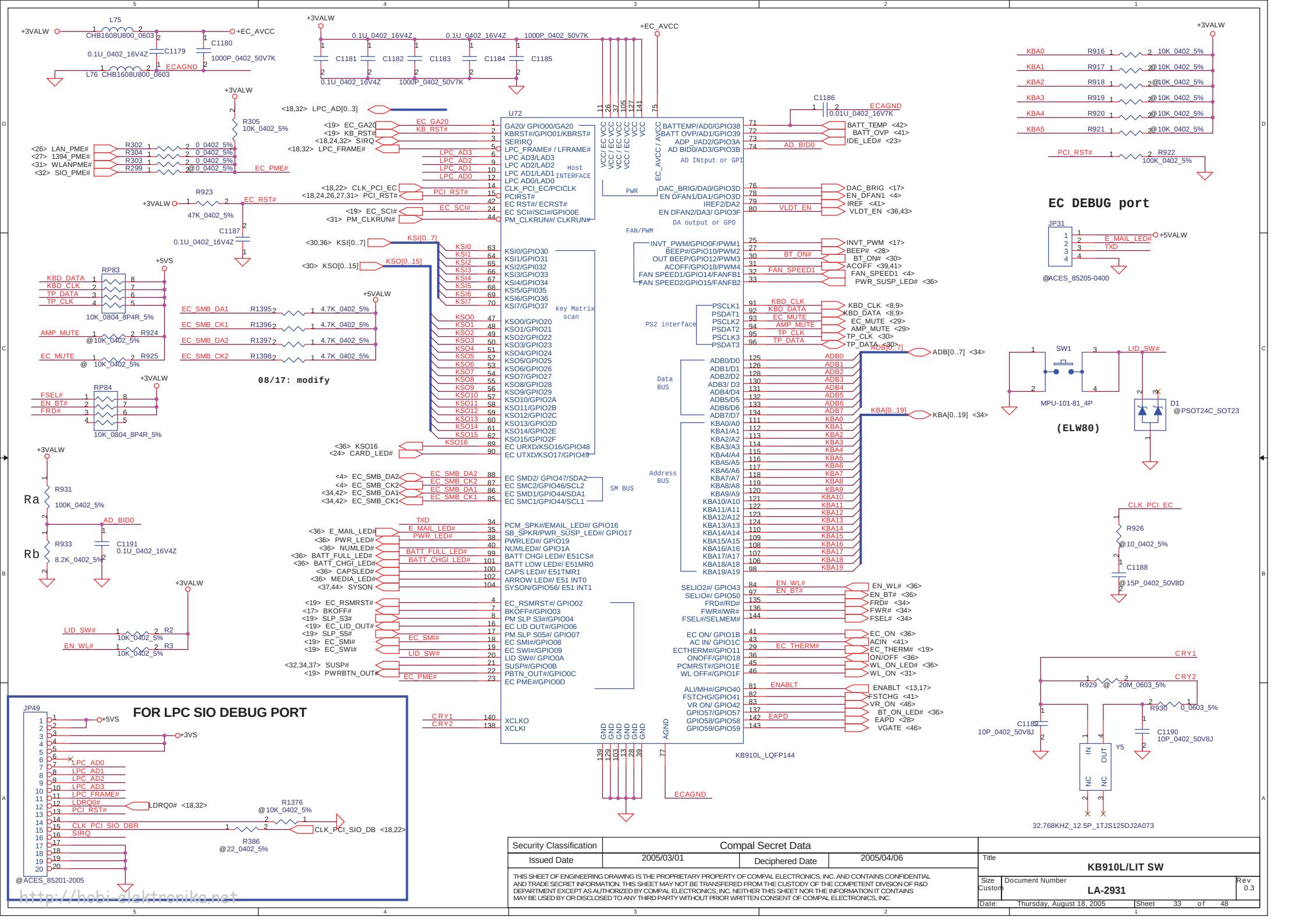

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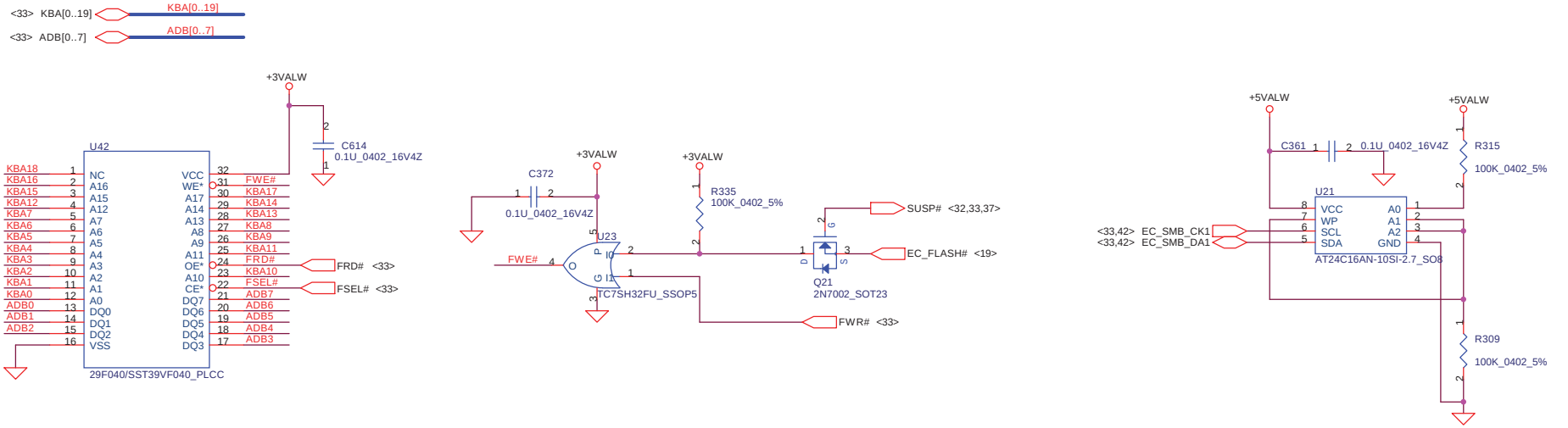
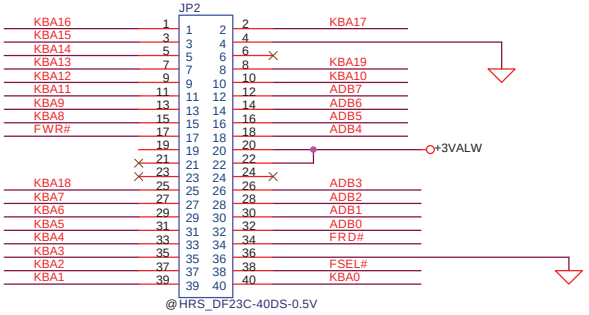


Bios Rom Chip Daughter Card



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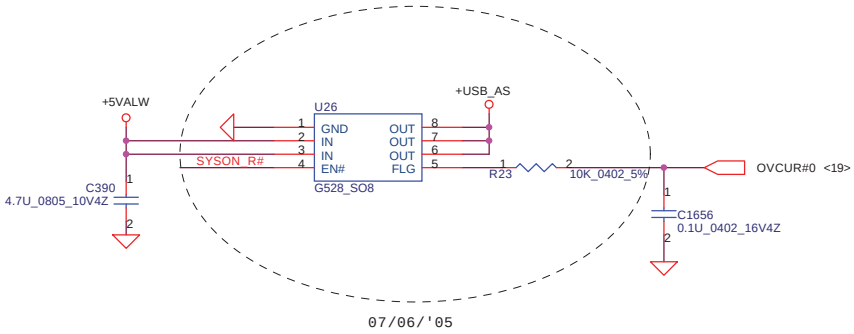

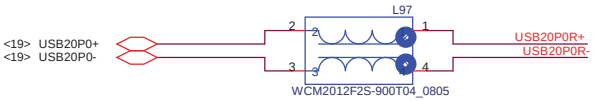

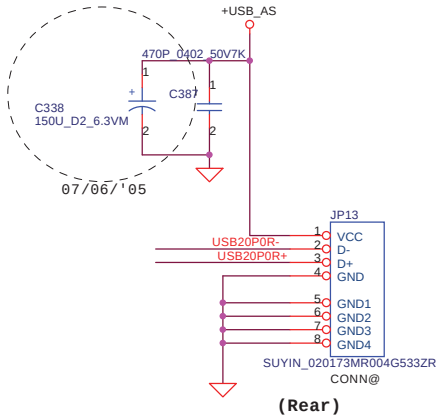

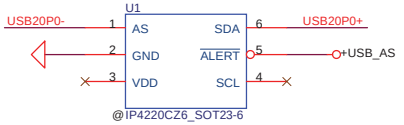

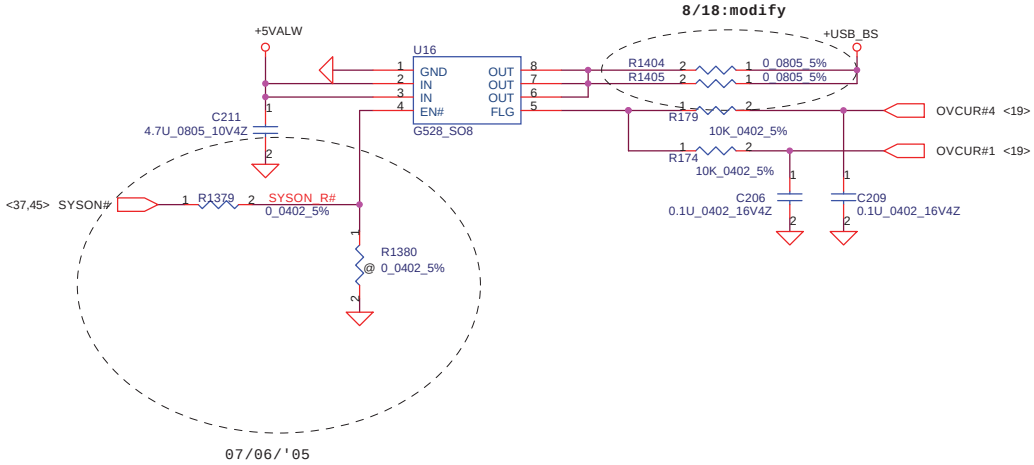

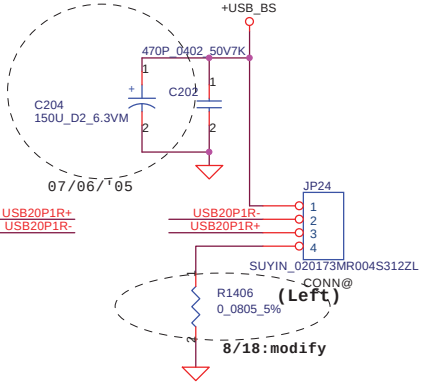

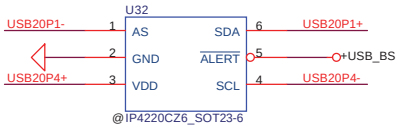

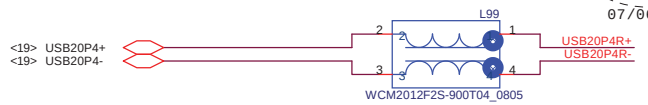

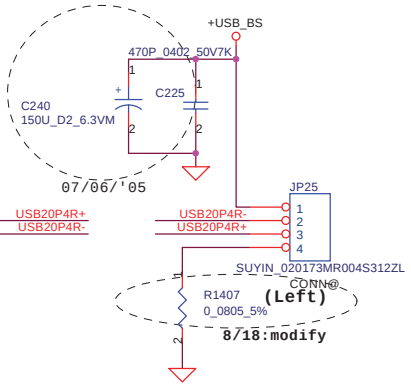

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Title	USB 2.0 Conn		
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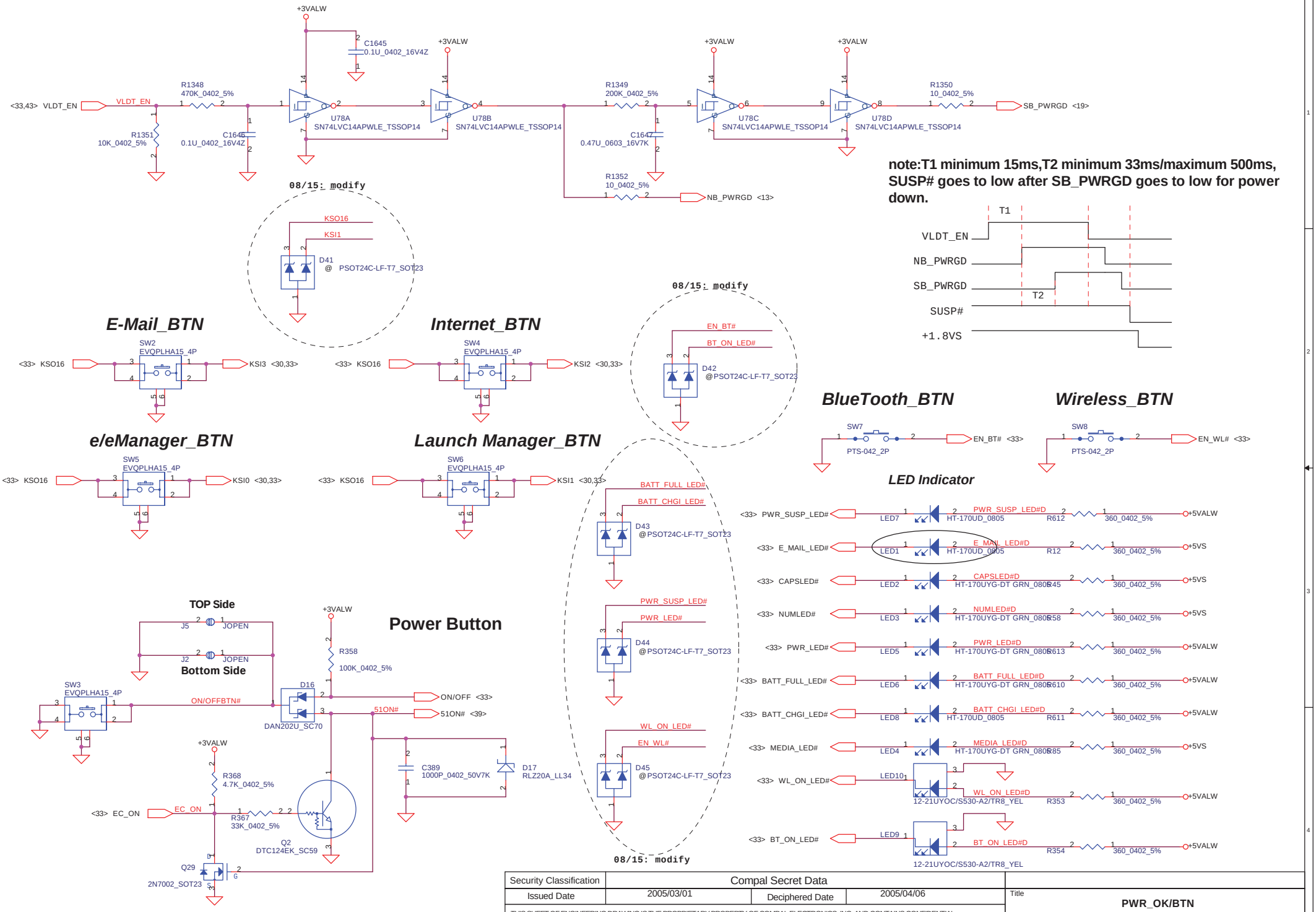

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Title	PWR_OK/BTN		
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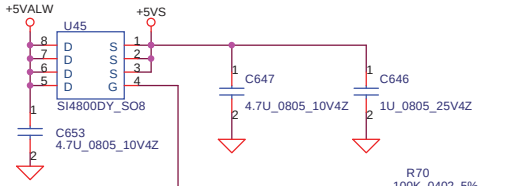
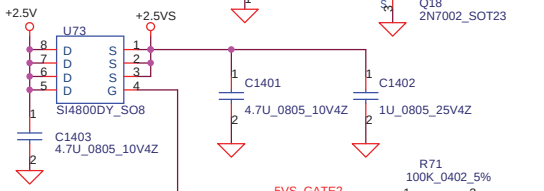
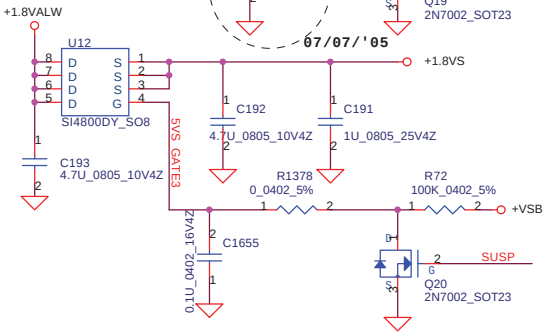
+5VALW TO +5VS



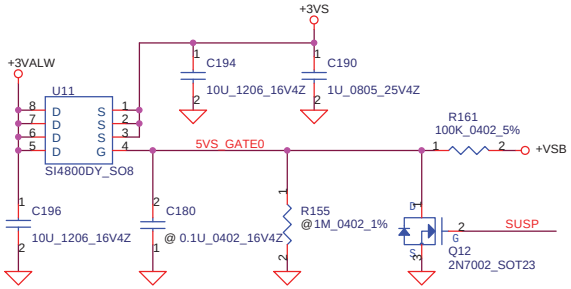
+2.5V TO +2.5VS

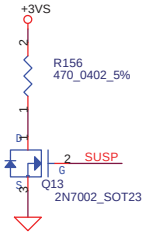


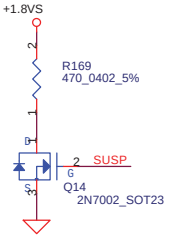
+1.8VALW TO +1.8VS

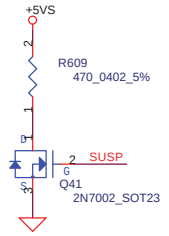


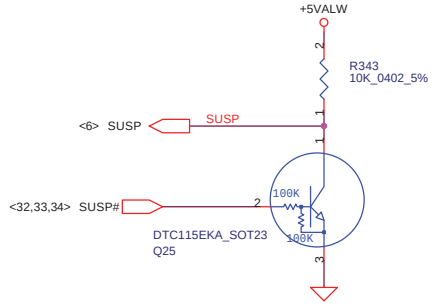
+3VALW TO +3VS

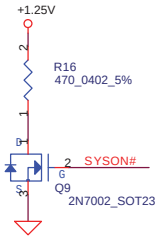


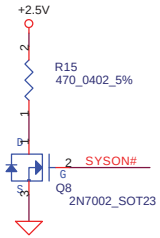


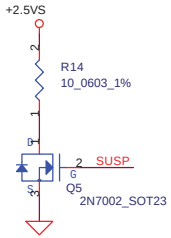


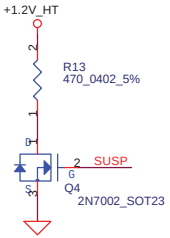


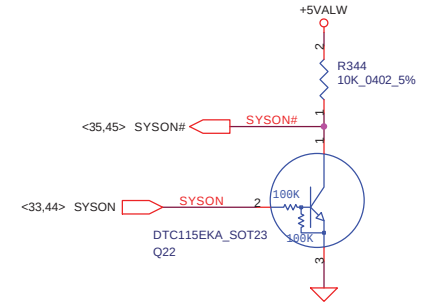












PROPRIETARY NOTE

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Title	DC Interface	
Size: B	Document Number: LA-2931	Rev: 0.3
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CF1 SMD40M80
CF8 SMD40M80
CF14 SMD40M80
CF16 SMD40M80
CF15 SMD40M80
CF2 SMD40M80
CF3 SMD40M80
CF6 SMD40M80
CF5 SMD40M80
CF4 SMD40M80
CF13 SMD40M80
CF7 SMD40M80
CF9 SMD40M80
CF10 SMD40M80

FD3 FIDUCAL
FD6 FIDUCAL
FD1 FIDUCAL
FD4 FIDUCAL
FD2 FIDUCAL
FD5 FIDUCAL

H1 H_S354D118
H23 H_S354D118
H20 H_S354D118
H19 H_S354D118
H18 H_S354D118
H16 H_C197D118
H17 H_C315D165
H12 H_R354X348D118
H21 H_S354D118
H7 H_S354D118
H14 H_S354D118
H2 H_C276D173
H5 H_C276D173
H15 H_C315D315N
H4 H_O335X236D256X157
H6 H_C394BC217D177
H13 H_C394BC217D177
H10 H_C394BC217D177
H11 H_C394BC217D177
H3 H_S433D118
H9 H_R551X350D165
H8 H_S354D165
H22 H_S429D157
H25 H_C394BC217D177
H26 H_O95X52D75X32
H27 H_C197D118
H28 H_C394BC217D177
H29 H_C394BC217D177

Chip_Name	Label_Name
EXP_TXP0/SDVOB_RED	PCIE_MTX_C_GRX_P0
EXP_TXN0/SDVOB_RED#	PCIE_MTX_C_GRX_N0
EXP_TXP1/SDVOB_GREEN	PCIE_MTX_C_GRX_P1
EXP_TXN1/SDVOB_GREEN#	PCIE_MTX_C_GRX_N1
EXP_TXP2/SDVOB_BLUE	PCIE_MTX_C_GRX_P2
EXP_TXN2/SDVOB_BLUE#	PCIE_MTX_C_GRX_N2
EXP_TXP3/SDVOB_CLKP	PCIE_MTX_C_GRX_P3
EXP_TXN3/SDVOB_CLKN	PCIE_MTX_C_GRX_N3
EXP_RXP1/SDVO_INT	PCEI_GTX_C_MRX_P1
EXP_RXN1/SDVO_INT#	PCEI_GTX_C_MRX_N1

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Security Classification	Compal Secret Data		
Issued Date	2005/03/01	Deciphered Date	2005/04/06

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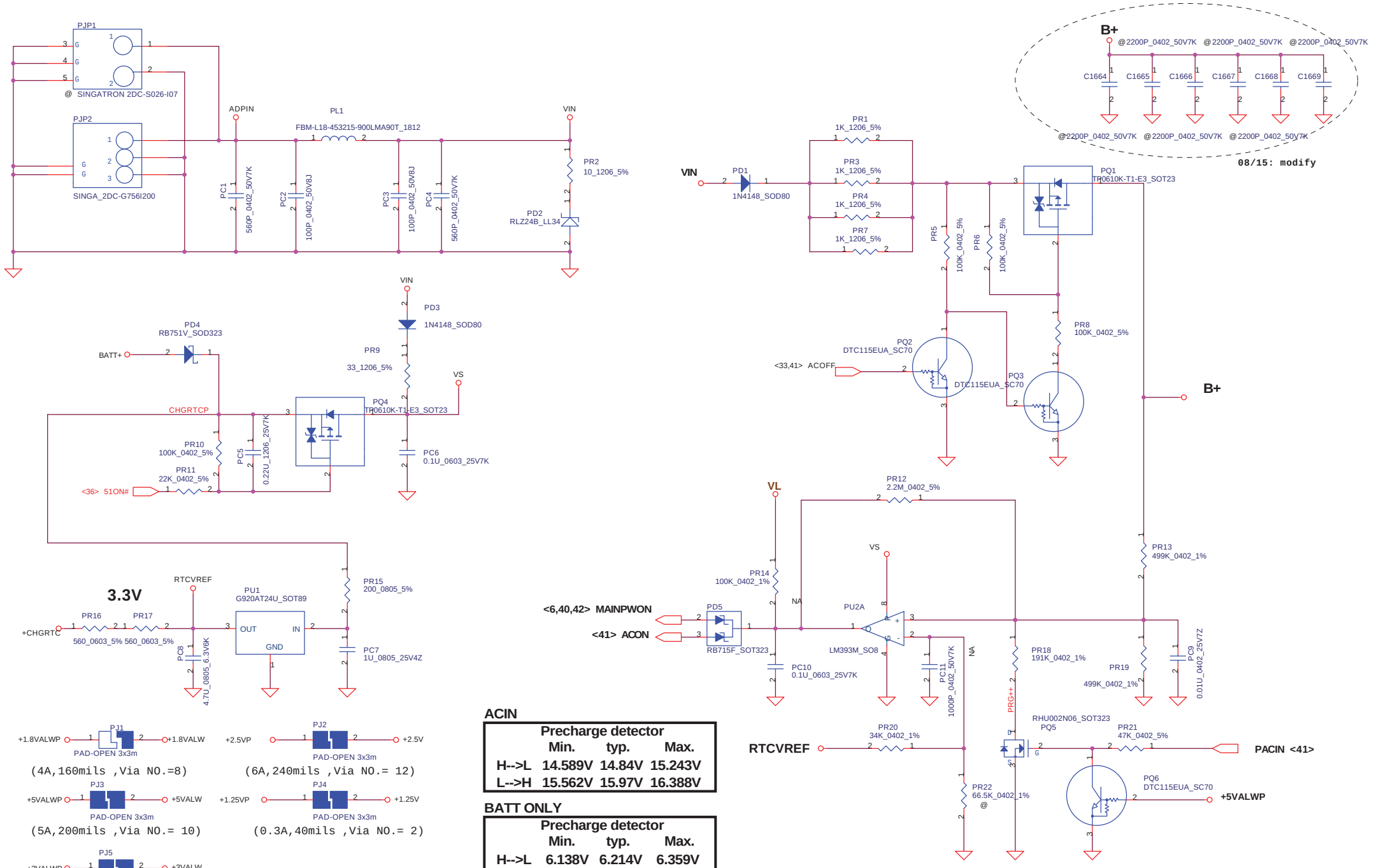
Title: **Screws**

Size: Custom | Document Number: **LA-2931** | Rev: 0.3

Date: Thursday, August 18, 2005 | Sheet 38 of 48



ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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Issued Date	2005/05/10	Deciphered Date	2006/05/10

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Compal Electronics, Inc.

Title	DCIN/DECTOR		
Size B	Document Number		Rev 0.3
Date: Thursday, August 18, 2005	Sheet 39 of 48		

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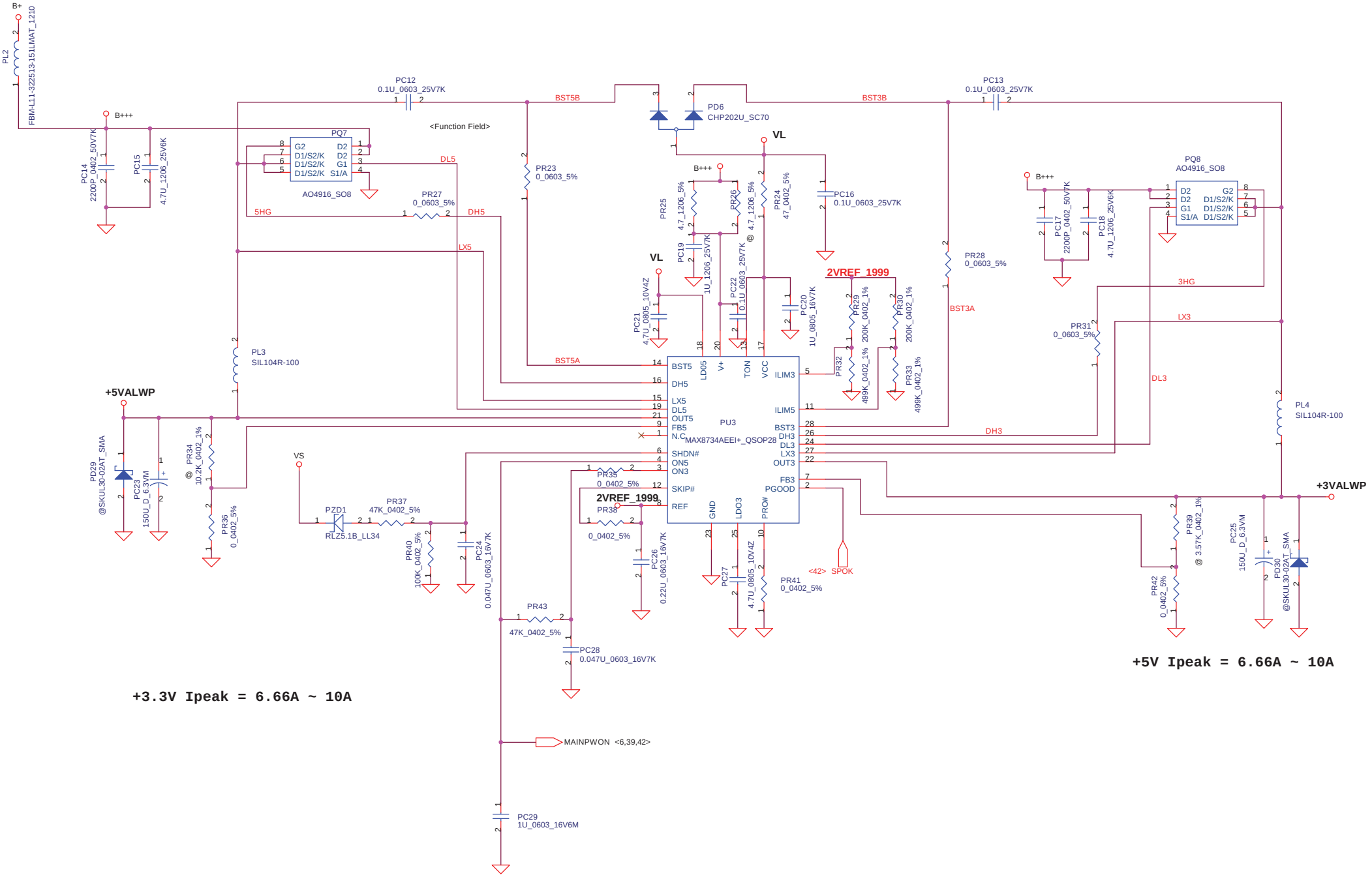

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Issued Date	2005/05/10	Deciphered Date	2006/05/10

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Compal Electronics, Inc.

Title: +5VALWP/+3VALWP

Size	Document Number	Rev
Custom		0.3

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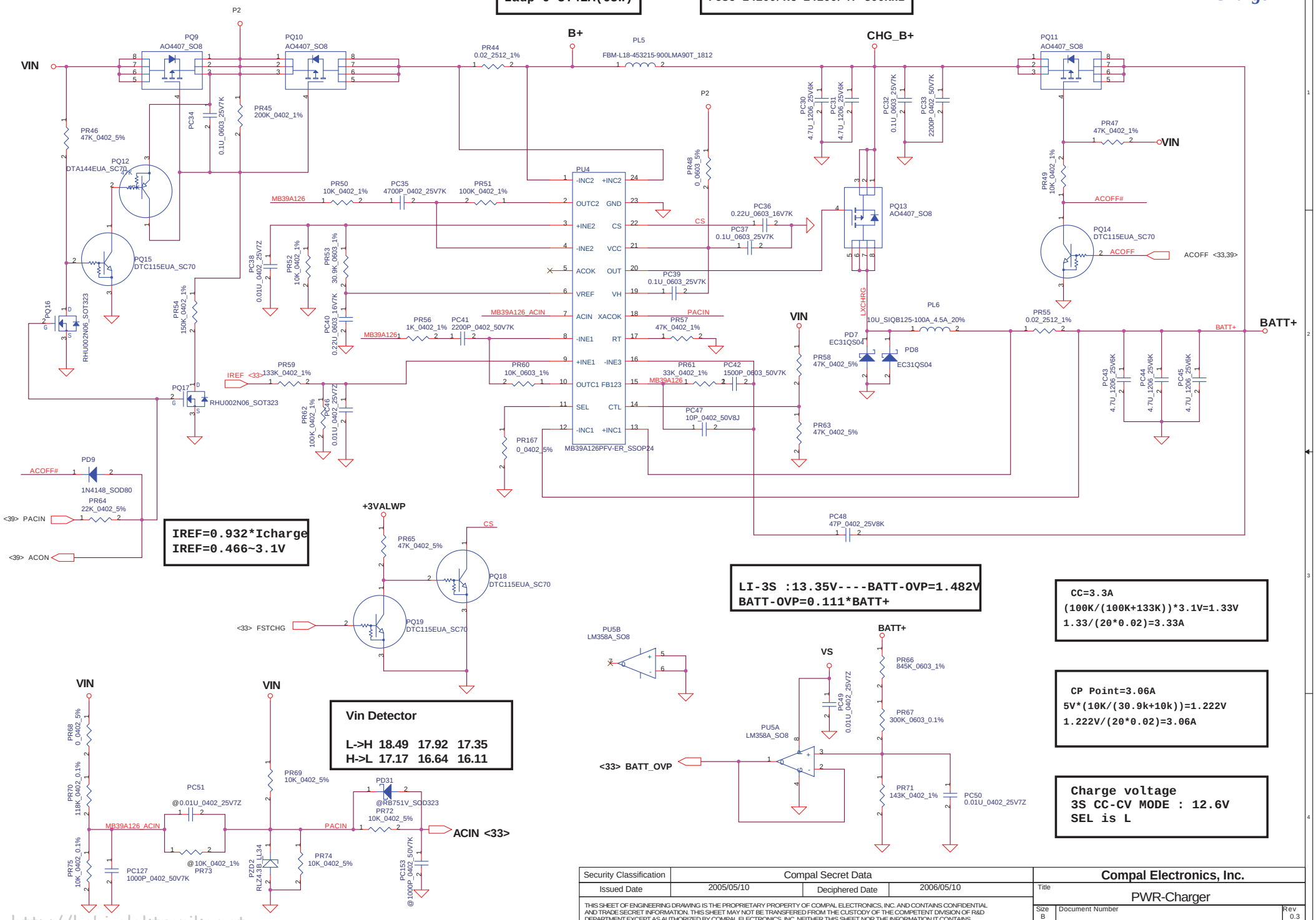
Charger

Iadp=0~3.42A(65W)

Fosc=14100/Rt=14100/47=300KHz



IREF=0.932*Icharge
IREF=0.466~3.1V

LI-3S :13.35V----BATT-OVP=1.482V
BATT-OVP=0.111*BATT+

CC=3.3A
(100K/(100K+133K))*3.1V=1.33V
1.33/(20*0.02)=3.33A

CP Point=3.06A
5V*(10K/(30.9k+10k))=1.222V
1.222V/(20*0.02)=3.06A

Charge voltage
3S CC-CV MODE : 12.6V
SEL is L

Vin Detector

L->H	18.49	17.92	17.35
H->L	17.17	16.64	16.11

Security Classification	Compal Secret Data		
Issued Date	2005/05/10	Deciphered Date	2006/05/10

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Compal Electronics, Inc.

Title: PWR-Charger

Size: B | Document Number | Rev: 0.3

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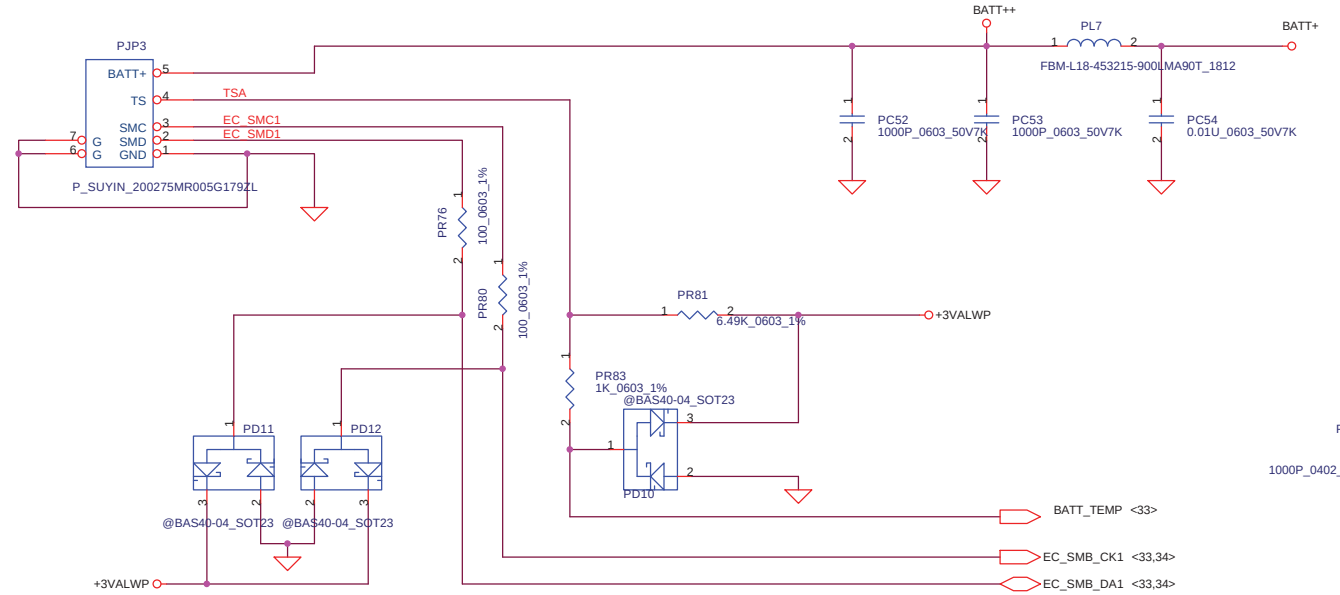
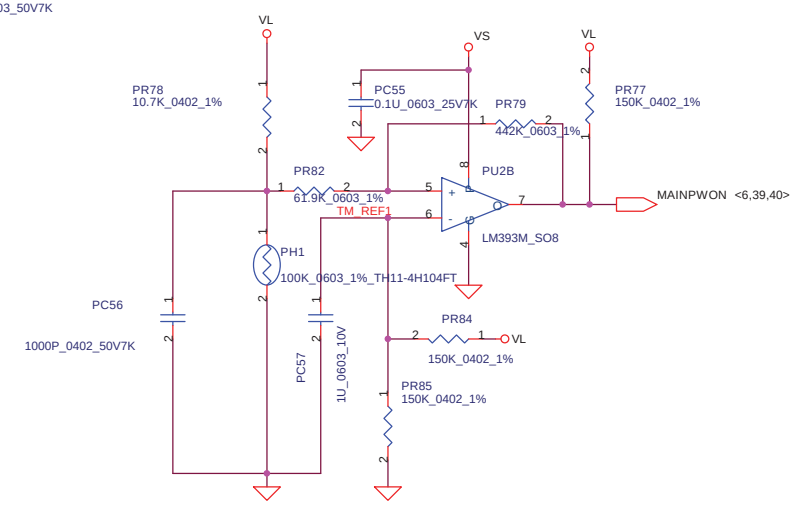
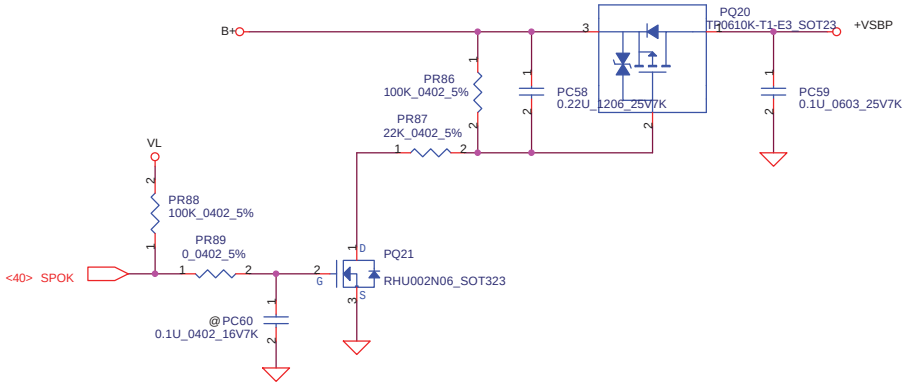


PH1 under CPU botten side :
CPU thermal protection at 85 degree C
Recovery at 70 degree C





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Compal Electronics, Inc.

Title: BATTERY CONN. / OTP

Size: B | Document Number | Rev: 0.3

Date: Thursday, August 18, 2005 | Sheet 42 of 48

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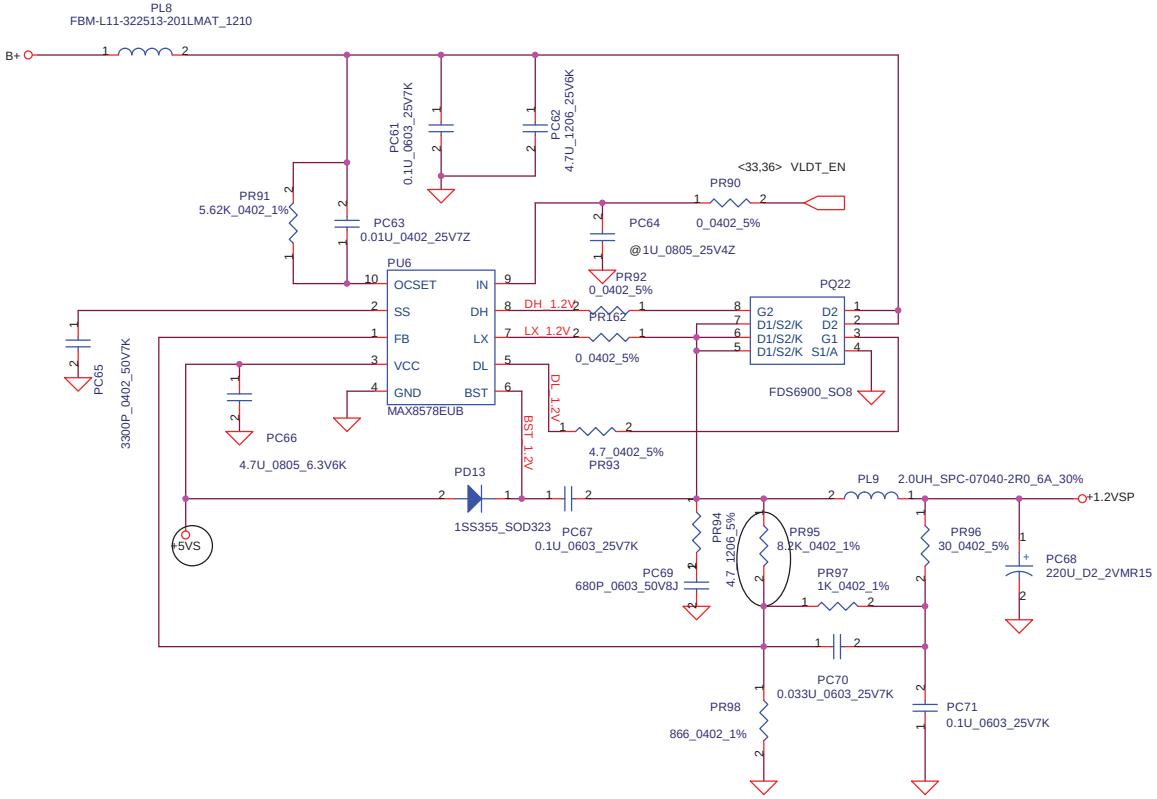
+1.2VSP Current limit = 8.29A ~9.6A



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Issued Date	2005/05/10	Deciphered Date	2006/05/10

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Compal Electronics, Inc.

Title	+1.2VSP	
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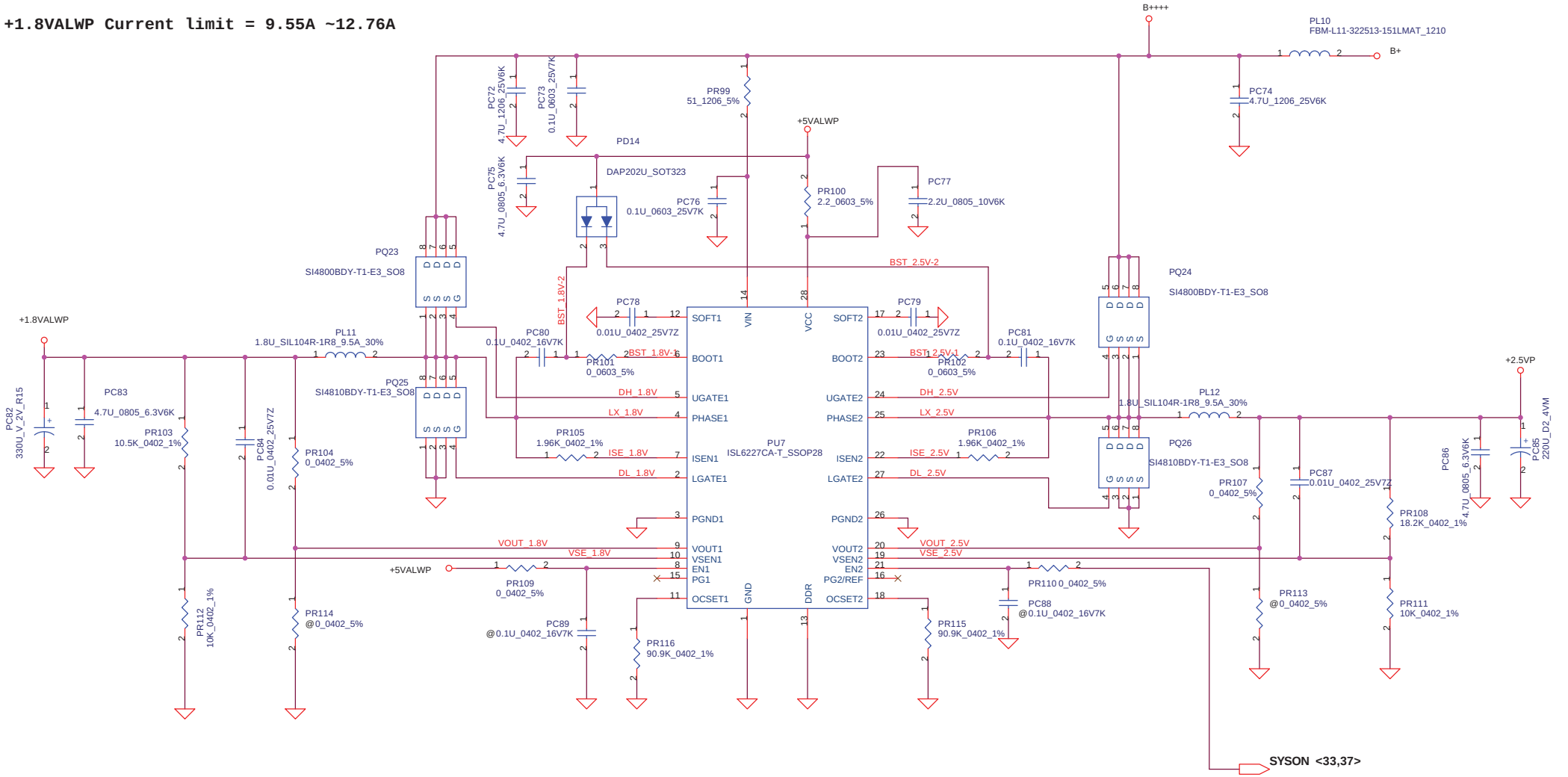
+2.5VP O.C.P. =9A ~ 12.2A

+1.8VALWP Current limit = 9.55A ~12.76A



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Compal Electronics, Inc.

Title: +1.8VALWP/+2.5VP

Size: B | Document Number | Rev: 0.3

Date: Thursday, August 18, 2005 | Sheet 44 of 48

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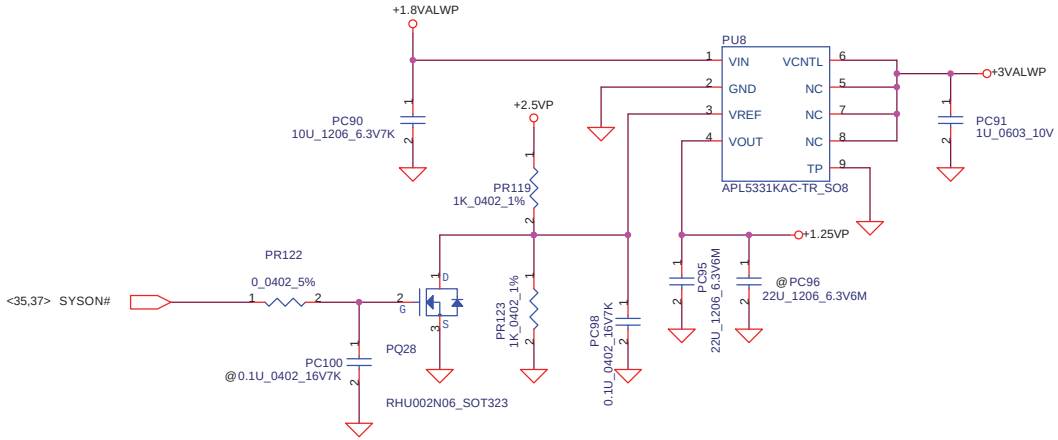

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Issued Date	2005/05/10	Deciphered Date	2006/05/10

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Compal Electronics, Inc.

Title: +1.25VSP/+1.5VSP

Size	Document Number	Rev
B		0.3

Date: Thursday, August 18, 2005 | Sheet 45 of 48

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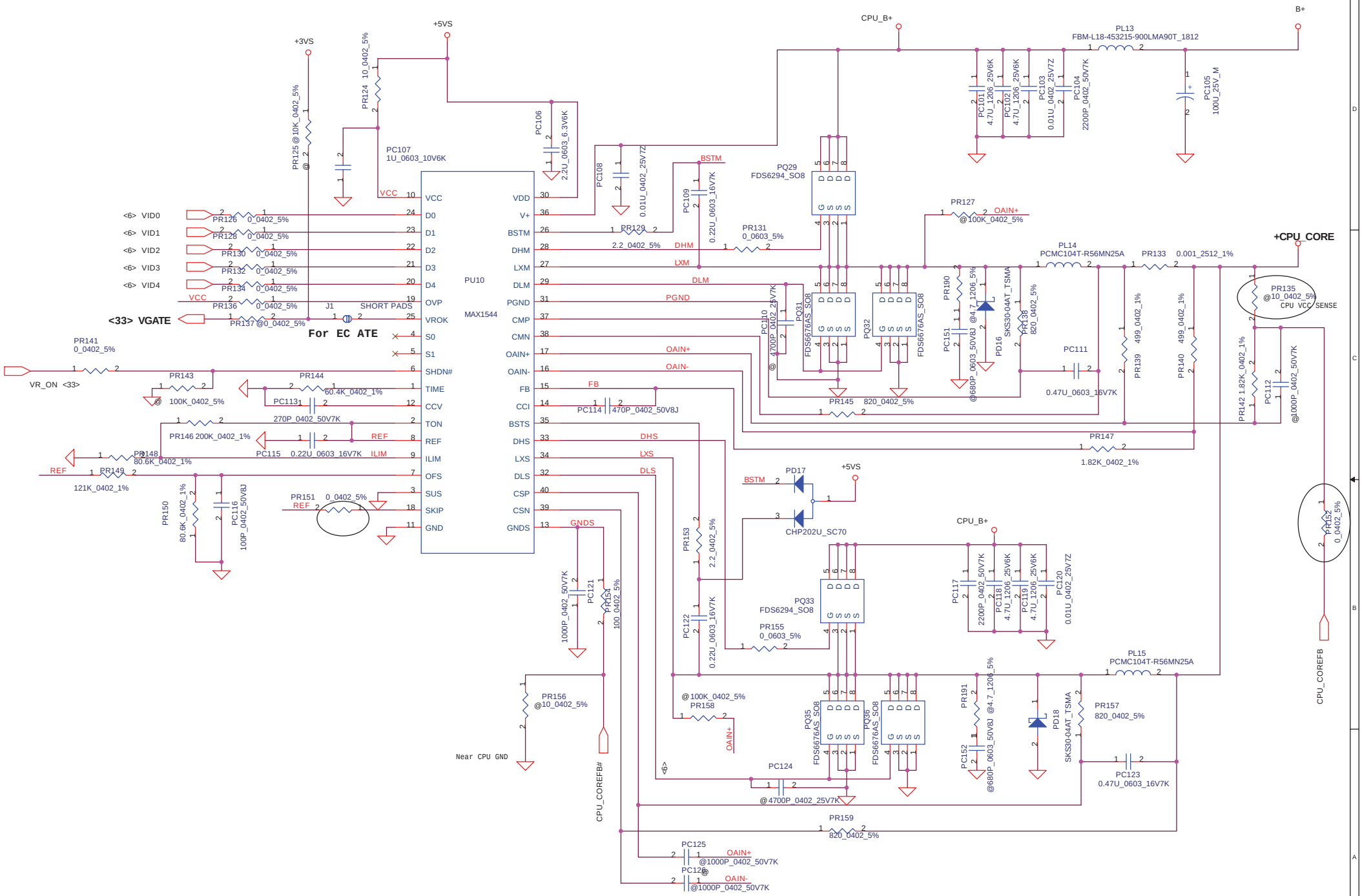

Security Classification	Compal Secret Data		
Issued Date	2005/05/10	Deciphered Date	2006/05/10

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Title	+CPU_CORE		
Size: Custom	Document Number		Rev: 0.3
Date: Thursday, August 18, 2005	Sheet 46 of 48		

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		add ACIN detect RC filter		42	add PD31,PC153		DVT
2		reverve or decrease CPU CORE ring with EMI solution : snubber		47	Reserve PR190//PR191: 4.7 1206 ,add PC151/PC152:680P		DVT
3		Modify 1.2VP voltage level		44	change PR95 from 6.81k to 8.2k		DVT
4		delete 1.2VP power good		44	delete PR164,PR163,PR165,PR166,PQ38,PQ39,PC128		DVT
5		delete Charger 3S/4S selector		42	delete PR160,PQ37		DVT
6							
7							
8							
9							
10							
11							
8							
9							

Compal Electronics, Inc.		
Title: PIR (PWR)		
Size	Document Number: LA-2931	Rev: 0.3
Date: Thursday, August 18, 2005	Sheet 47 of 48	

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1	1.Del +3V PWR		0.2	30,31			
2	1.Del Q3,C611,C609,C639,R341,Q24,R340		0.2	37			
3	1.Del JP6 2.PWR_SUSP_LED#/WL_ON_LED#/BT_ON_LED# conn to EC		0.2	36			
4	1.Del NET MSPWREN# 2.Del R561/R634 3.Change XDOC# to MSOC#		0.2	24/25			
5	1.change LAN LED PWR from +2.5V_LAN to +3VALW 2.DEL R856 3.Change Q52		0.2	26			
6	1.DEL MIC1 2.Change Q38		0.2	29			
7	1.Change U26 to G528 2.ADD C1656/R1379/R1380/L97/L98/L99/R1381~R1386		0.2	35			
8							
9							

Security Classification: Compal Secret Data
Issued Date: 2005/03/08 Deciphered Date: 2006/03/08

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Title: PIR (HW)
Size: Custom | Document Number: EFL50 LA-2761 | Rev: 0.3
Date: Thursday, August 18, 2005 | Sheet 48 of 48

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